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Design of DC-DC Buck Converter for Smartphone Applications Based on FPGA Digital Voltage Controller

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Abstract— *This paper presents an enhancement of the output performance of a linear buck converter system for the mobile (smartphone) devices using an adaptive digital Proportional–Integral–Derivative (PID) controller with off-line swarm optimization algorithm. The work focuses on improving the use of using single-input single-output (SISO) digital Field Programmable Gate Array (FPGA)-PID to control the linear buck converter system. The goal of the proposed adaptive SISO-FPGA-PID voltage-tracking controller is to rapidly and precisely identify the optimal voltage control action (optimal on-off duration time) that is used to control the buck converter output voltage level in order to avoid the troubleshooting hardware problem issues on mobile devices. The Particle Swarm Optimization (PSO) algorithms are used to find and tune the three weights of the SISO-FPGA-PID controller. The numerical simulation results and the experimental work using Spartan-3E xc3s500e-4fg320 board with Verilog hardware description language (HDL) show that the proposed controller is more accurate in terms of voltage error and the number of function evolutions are of high reduction. As well as to generate a smooth voltage control response without voltage oscillation in the output by investigating under mobile applications variations such as using Bluetooth, WI-FI, and CPU operating voltage when these results are compared with other controllers.*

Index Terms— *Buck Converter System; Adaptive SISO-FPGA-PID Controller; Off-Line Particle Swarm Optimization.*

I. INTRODUCTION

Mobile clients spend larger part of their time utilizing the mobile applications (apps). These mobile applications are designed and allocated for internet access, communications, scheduling, data transferring, entertainment and many more applications that make the smartphones critical and essential in users' day-to-day activities. Many different mobile applications are designed to be able to be accessed and used by mobile user simultaneously. Moreover, the usefulness and complexity of the mobile apps require more resources from the mobile phone. These involve higher CPU utilization, more memory utilization and speedier wireless communication radio, [1]. These applications consist of software and hardware. Thus, for viable utilization of mobile devices distinctive applications ought to be with enhanced and fully optimized performance in terms of quickly power delivered and keeping on precisely voltage level during using these applications, in order to avoid the troubleshooting hardware problem issues on mobile devices. In this way, designing and controlling the switching circuits for "DC-DC power converter" responsible for the battery operation are needed to attain the regulation of voltage for quick transient response with high efficiency of conversion, [2]. The DC-DC converters are the most power electronic circuit that changes main sources of direct current (DC) from one voltage level to another voltage level by switching activity. This will be done by altering the duty cycle of the main switches within the control circuits. The switches are active transistors. These converters are a generally utilized as regulated switched mode power supplies, which converts the unregulated DC input to a regulated DC output, [3].

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The control and stabilization of switching converters are the essential factors that ought to be a considered. Therefore, the motivation of this work is appropriate control strategy must bargain with the dynamic behavior dilemmas of DC-DC converters, which influence the work of mobile devices. These dilemmas are epitomized by the variation in the output voltages; the wide scale of loading current; uncertain model parameters and the levels variation in input voltage, [2], [4].

In the related literature, numerous researchers exploit robust control methodologies in order to keep up with the demanded control objectives. In this context, the predictive controller to ensure a tight regulation of the output voltage that led to stabilize the buck converter output was suggested in [5]. The PI-Lead controller is used to regulate the output voltage of buck converter through tuning the parameters of controller in two parts, PI part enhance the steady state response and Lead part enhance the transient response of unregulated system that was proposed in [6]. In addition, the studied Hysteresis Controller was proposed in [7] to achieve the required fast transient control unit, which enabled the controller to respond to the output voltage deviation rapidly and to control the timing of the bandwidth adjustment. Also, the back-stepping controller by depending on the dynamical model of buck converter in order to provide good robustness against outer disturbances and improve the performance of rapidly tracking to the output voltage response was presented in [8]. The exhibited fuzzy logic controller to achieve a stable and fast speed response of the buck converter system through evaluating and obtaining best control action as pulse width modulation (PWM) and altering continuously duty cycle until reaching the desired output voltage without a need to the buck converter mathematical model was explained in [9]. Furthermore, the sliding mode controller that achieved the stability and robustness of the system parameters in the presence of unexpected load and input voltage variations with constant frequency was proposed in [10].

This paper focuses on optimizing the dynamic responses of the buck converter output voltage and stabilizing its power output, particularly when different loads are employed in mobile applications. However, representative modelling of the buck converter system and control of the output voltage remain challenging issues. This paper provides the following:

- An analysis of the buck converter operating system with respect to the effect of each variable parameters, such as capacitor resistor, indictor resistor and the load current.
- A feedback SISO-PID controller is designed for the use in stabilizing and tracking the desired output voltage of the buck converter system in a transient state with variable Smartphone applications such as Bluetooth, Wi-Fi, as well as CPU operating voltage, in addition to obtaining optimal (or near optimal) voltage control action using off-line tuning swarm algorithm.
- A digital SISO-FPGA-PID control law is designed, implemented and verified using a FPGA Spartan-3E Starter kit xc3s500e-4fg320 device with Verilog hardware description language in real-time MATLAB environment system.

This paper is arranged as follows: Section 2 explains the modelling of the buck converter system; Section 3 presents the SISO-FPGA-PID controller using off-line particle swarm optimization algorithm; Section 4 discusses the numerical results of simulations conducted using the proposed controller; Section 5 demonstrates the experimental work based on Spartan 3E Starter kit; and Section 6 gives conclusions made with respect to the proposed controller.

II. BUCK CONVERTER MATHEMATICAL MODEL

The DC-DC Buck converter can be classified into the Step down or Chopper circuits. In fact, the output voltage (Vo) of the buck converter is less than input voltage source (Vg), because the input voltage source (Vg) is stepping down through the factor (Δ), [11]. Having a precise and complete model, which contains all the system parameters (such as the active switch turn-on resistance, inductor and capacitor resistance) is the main step in designing a non-conservative robust controller for Buck convertors. So that in this work, all parasitic resistance of elements are considered in order to obtain more accurate model, [12]. As shown

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in Fig. 1, the buck converter circuit consists of two active n-channel MOSFETs power (Q1) for switch and (Q2) for synchronous rectifier, main inductor (L), main capacitor (C), load resistance (R), input voltage source (Vg), output voltage (Vo), capacitor voltage (Vc), and inductor voltage (VL).

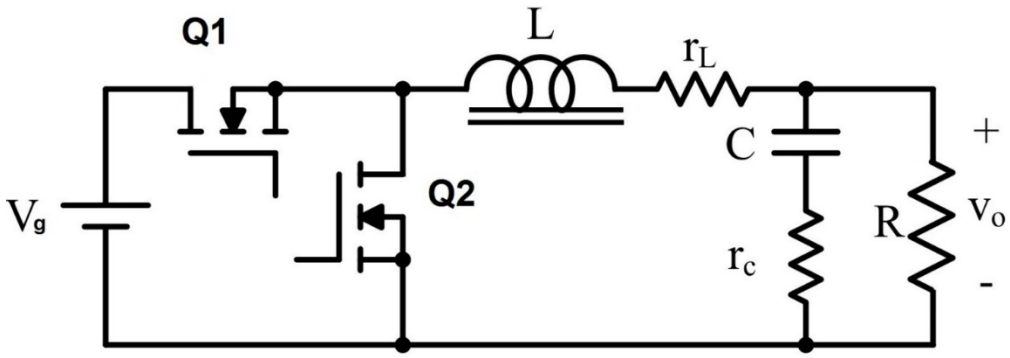

FIG. 1. POWER CIRCUIT DIAGRAM OF A SYNCHRONOUS DC-DC BUCK CONVERTER.

- In circuit of Fig. 1, there are two states; the ON and OFF time states. The on time is indicated by ΔT=T1, and the off time is indicated by (1-Δ)T=T2, where T=T1+T2.
- During On State when Q1 is on and Q2 is off, at a time period t<T1, and by applying Kirchhoff's voltage law, the circuit analysis can be described as follows:

$$V_g - i_L \cdot rs_{on} - L\frac{di_L}{dt} - i_L \cdot r_L - V_o = 0 \quad (1)$$

- During OFF State when Q1 is off and Q2 is on, at a time period T1<t<T2, and by applying Kirchhoff's voltage law the circuit analysis can be described as follows:

$$- i_L \cdot rs_{on} - L\frac{di_L}{dt} - i_L \cdot r_L - V_o = 0 \quad (2)$$

By defining Δ as in (3). Which turns (V_g) on-off as switching function.

$$\Delta = [o \quad to \quad 1] \quad (3)$$

Then (1) will be as follows:

$$\Delta V_g - i_L \cdot rs_{on} - L\frac{di_L}{dt} - i_L \cdot r_L - V_o = 0 \quad (4)$$

Therefore, (2) and (4) are formed in state space representation as follows:

Let $x_1 = i_L$ then $\dot{X}_1 = \frac{di_L}{dt}$, $x_2 = V_o$ then $\dot{X}_2 = \frac{dv_o}{dt}$ (5)

$$\dot{X} = A \cdot X + B \cdot V_g \quad , Y = C \cdot X \quad (6)$$

$$A = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} = \begin{bmatrix} \frac{-(rs_{on}+rl)}{L} & -\frac{1}{L} \\ \frac{LR-CRrc(rs_{on}+rl)}{LC(R+rc)} & \frac{-CRrc-L}{LC(R+rc)} \end{bmatrix} \quad (7)$$

$$B = [b_1 \; b_2] = \left[\frac{\Delta}{L} \quad \frac{Rrc}{L(R+rc)}\right] \cdot V_g \quad (8)$$

$$C = [0 \quad 1] \quad (9)$$

Finally, the continuous-time transfer function of the buck converter model can be expressed as follows:

$$\frac{Y(s)}{(s)} = V_g \frac{\frac{Rrc}{L(R+rc)}S + \frac{R}{Lc(R+rc)}}{s^2 + \left(\frac{rs_{on}+rl}{L} + \frac{L+CRrc}{LC(R+rc)}\right)s + \frac{R+rs_{on}+rl}{LC(R+rc)}} \quad (10)$$

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III. An ADAPTIVE SISO-FPGA-PID CONTROLLER DESIGN

The control methods such as proportional integral derivative (PID) and algorithms are one of the most important types of effective feedback controllers, which are utilized in many industrial automatic control processes. PID controller has been vastly used in numerous different scopes, such as mechatronics, power systems, drives control, process control, aerospace, and robotics, [13], [14]. PID controller has time domain regulation and good closed loop response, [15]. Fig. 2 illustrates the block diagram of suggested adaptive SISO-PID controller based off-line self-tuning control algorithm**,** which has a big dynamic characteristic, high adaptation and rugged "robustness" performance because of its capability in tuning and finding the control gains of PID controller.

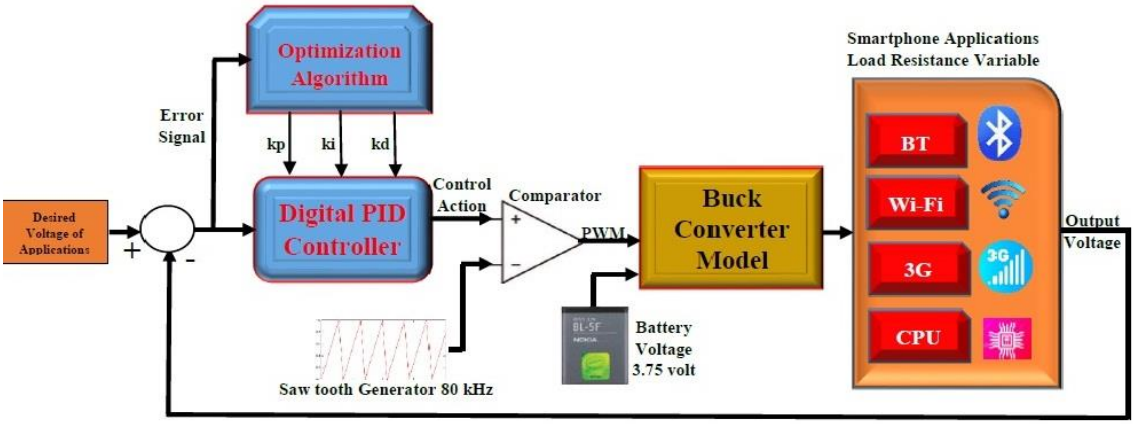

FIG. 2. AN ADAPTIVE DIGITAL SISO-PID CONTROLLER BLOCK DIAGRAM FOR BUCK CONVERTER OF SMARTPHONE APPLICATIONS.

The control operation U(s) of the suggested "off-line self-tuning adaptive PID controller" is very essential for stabilizing the error voltage signal E(s) for the output of buck converter system to avoid the eroding of output voltage Y(s) from the offset voltage Vd(s) and to satisfy a great rating of performance for disturbance repudiation and ambiguous parameters. From **[**6], the time-domain form of PID controller written as follows**:**

$$u(t)=K_p\ e(t) + K_i \int_0^t e(t)\ d(t) + K_d \frac{de(t)}{dt} \quad (11)$$

The continuous controller (PID) in (11) is transformed to digital equivalent form as in (12) by using z-transform for implementing the adaptive PID controller in field programmable gate arrays (FPGA), where the integration and differentiation are implemented numerically with backward difference respectively.

$$U(z)= [K_p + \frac{K_i\ T_s}{1}\frac{1}{1-Z^{-1}} + K_d \frac{1-Z^{-1}}{T_s}]\ E(z) \quad (12)$$

Where: T_s is the sampling time at the k^{th} samples.
Moreover, the effective output $u(k)$ of the controller, described as follows:

$$u(k)= u(k-1) + K_p(e(k) - e(k-1)) + K_i\ e(k) + K_d\ (e(k) - 2\ e(k-1) + e(k-2)) \quad (13)$$

Then converting the (13) to a Verilog Hardware Description Language (HDL) program by using Integrated System Environment (ISE) package version 14.7 and it has taken an image to the Verilog program as in Fig. 3. Then using ISim simulator based on ISE package for simulation and testing the SISO-FPGA-PID controller program is verified as shown in Fig. 4.

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```
module siso_pid_fpga(
input clk,
input ce,
input signed [19:0] e,
input signed [19:0] ee,
input signed [19:0] eee,
input signed [19:0] kp,
input signed [19:0] ki,
input signed [19:0] kd,
output reg signed [19:0] pcont,
output reg signed [19:0] icont,
output reg signed [19:0] dcont,
output reg signed [19:0] action);

reg signed [19:0] pconttemp;
reg signed [19:0] etemp;
reg signed [19:0] eetemp;
reg signed [19:0] eeetemp;
reg signed [19:0] temp;
reg signed [19:0] utemp;
reg signed [19:0] uutemp;
reg signed [19:0] uu =0;

always @(posedge clk)
begin
action=uu;
etemp=(e-ee);
pcont=kp*etemp;
icont=ki*e;
eeetemp=e+eee;
eetemp=ee+ee;
temp=eeetemp-eetemp;
dcont=kd*temp;
utemp=pcont+icont;
uutemp=utemp+dcont;
action=uutemp+uu;
uu=action;
end
endmodule
```

FIG. 3. SISO-FPGA-PID VERILOG PROGRAM AFTER HAS TAKEN IMAGE FOR IT.

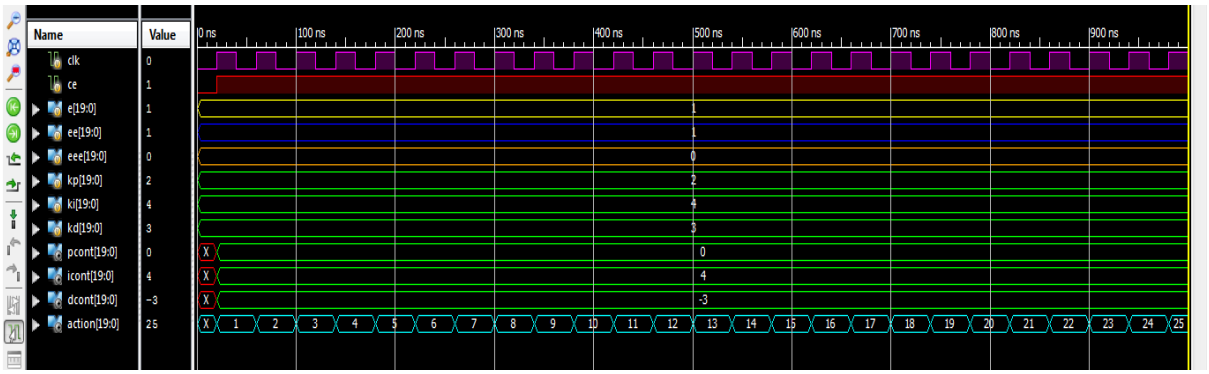

FIG. 4. SISO-FPGA-PID TESTING.

The intelligent off-line PSO algorithm is described in flowchart as shown in Fig. 5 that is used to illustrate the effectiveness of the algorithm in terms of the number of iterations employed, rating the fitness function and obtaining the minimum value for the cost function. These effectiveness lead to find and tune the best weights of the SISO-FPGA-PID controller to produce the good and pure voltage control operation that leads to fast track the desired output voltage of buck converter during load current variation when different application are used.

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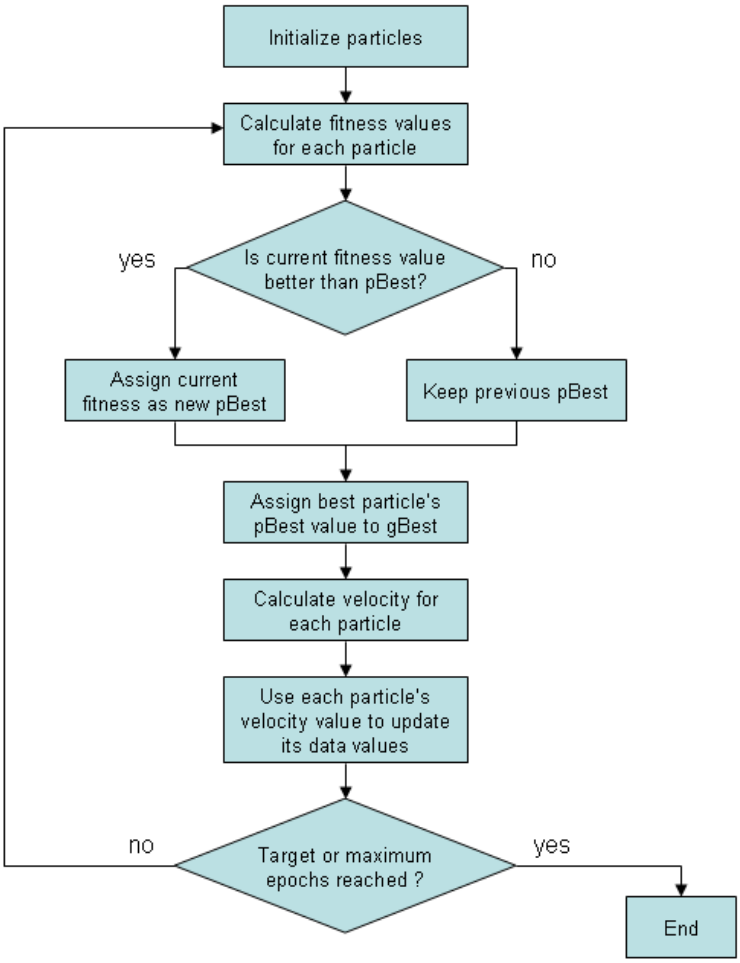

FIG. 5. FLOWCHART OF THE OFF-LINE PSO ALGORITHM.

The particle updates its velocity and positions with following equations: (14) and (15), which are obtained from [16], [17].

$$v = w \,.\, v + c_1 \,.\, r_1 \,.\, (l_{\_best} - y) + c_2 \,.\, r_2 \,(g_{\_best} - y) \quad (14)$$

$$y = y + v \quad (15)$$

Where, w is the inertia weighting factor for the velocity v; c_1 and c_2 are acceleration parameters and positive constants values; r_1 and r_2 are random values between 0 and 1; $l_{\_best}$ represents the best previous position visited by each individual particle and $g_{\_best}$ represents the position of the best point in search space visited by all swarm particles at yet.

The learning swarm algorithm usually based on minimization of the following off-line cost function,

$$E = \frac{1}{P}\sum_{i=1}^{p}[Vdes(k+1) - Vo(k+1))^2] \quad (16)$$

Where, *p* represents the number of training points in the training set; *Vo*(*k+1*) is the actual output voltage of the buck converter of each k[th] iterations $Vdes$(*k+1*) represents the desired output voltage of every iteration.

IV. MATLAB SIMULATION RESULTS

In this work, to carry out the proposed controller, the specifications of buck converter power circuit at switching frequency 80 kHz are obtained from, [2] and [18] as illustrated in Table 1.

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TABLE 1. ELECTRONICS COMPONENTS VALUES OF THE BUCK CONVERTER MODEL AT SWITCHING FREQUENCY 80 KHZ [2], [18].

Description	Symbol	Value	Unit
Inductance	L	47	μH
Capacitor	C	68	μF
Load Resistance	R_{load}	2.345	Ω
Inductor Effective Series Resistance	r_l	0.13	Ω
Capacitor Effective Series Resistance	r_c	55	m Ω
The ON-n-Channel Resistance of MOS Transistors	rs_{on}	2.1	Ω
Supply voltage	V-supply	3.75	V

Using MATLAB simulation (m.file) to implement the control algorithm PSO tuning with adaptive PID controller in off-line mode, to track the required voltage level in output of the DC-DC buck converter and at specific sampling time. From (10), the natural frequency W_n=2.44×10^4rad/sec and the damping ratio ζ= 1.12 of the buck converter model can be calculated , from this calculated two values the model time constant which is equal to τ=36.5μsec can be calculated and by depending on Shannon's theorem the sampling time can be calculated which is equal to 3.6μsec. The specifications in TABLE 1 are represented as difference equation as in (17).

$$v_o(k)= 0.02067\ u(k-1)- 0.007375\ u(k-2)+1.814\ v_o(k-1)-0.8212\ v_o(k-2) \quad (17)$$

Fig. 6. shows the dynamical behavior of the buck converter output voltage for unit step change open loop response, which has stable response, but it has high voltage error.

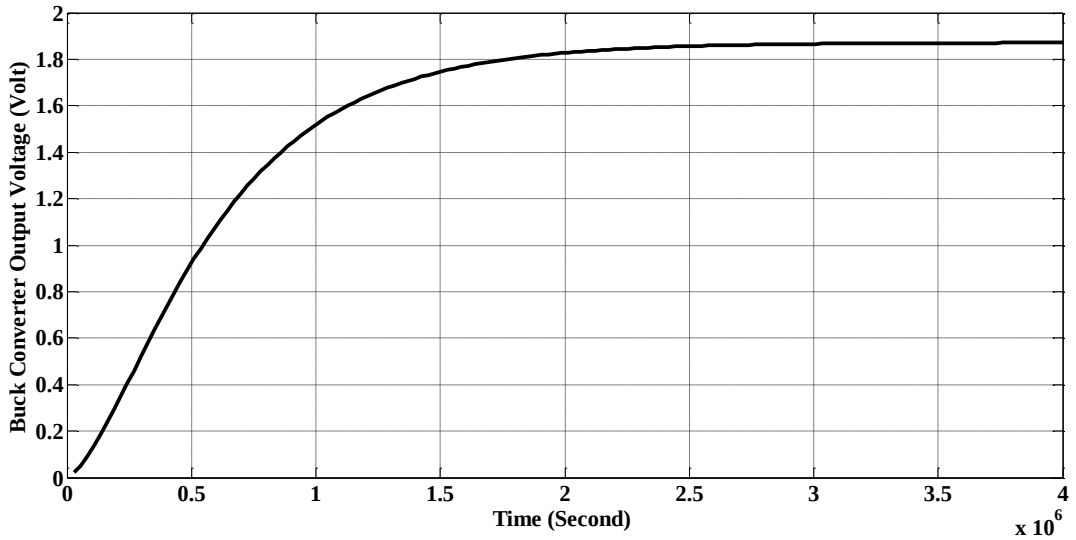

FIG. 6. OPEN LOOP RESPONSE FOR BUCK CONVERTER SYSTEM.

Based on Fig. 2, this is so to demonstrate the adaptive digital SISO-PID controller with off-line PSO tuning control parameters algorithm, which is defined as in, Table 2. The tuning swarm algorithm and at least number of iterations has the ability to fast producing perfect and pure voltage control operation and reducing the error in the actual output voltage.

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TABLE 2. THE SUGGESTED TUNING PARAMETER VALUES OF ALGORITHM.

Parameter	Value
No. of particles.	20
Max iteration No.	50
Acceleration constants, c_1, c_2	1.49, 1.49
Random No. r_1, r_2	[0,1]
Inertia weight, w	0.73

The specifications of smartphone applications for NoKia N95 that are taken from [19] can be demonstrated in Table 3. to show the equivalent resistance of each application that is represented as variable load at in buck converter output model.

TABLE 3. THE SPECIFICATIONS OF SMARTPHONE APPLICATIONS FOR NOKIA N95 [19].

Application	TTL low Level Voltage (V)	Full Current load (mA) And Consumption Power (mW)	Equivalent Resistance (Ω)
CPU	1.5	408mA, 612mW	3.676
Wi-Fi	2.5	580mA, 1450mW	4.31
Blue Tooth (BT)	2.5	172.8mA, 432mW	14.46

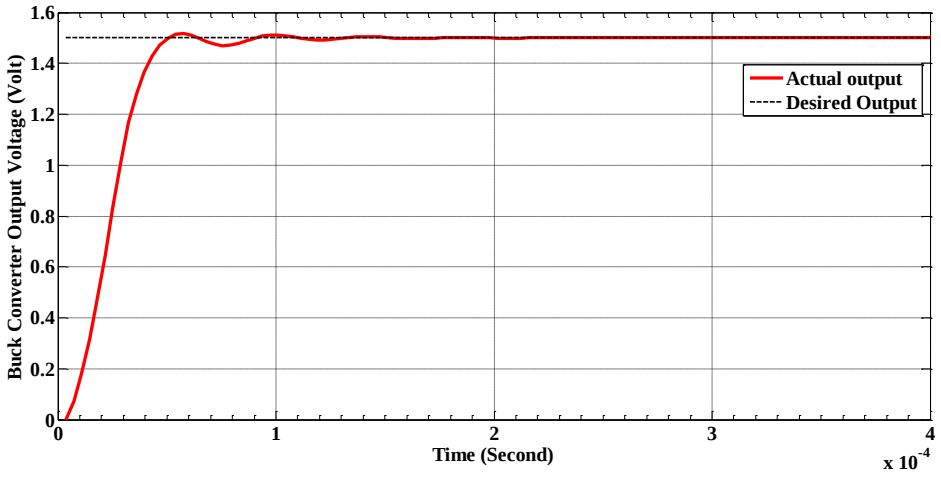
Case I

The difference equation of buck converter model for CPU application in the smartphone can be represented in Eq. (18).

$$v_o(k)= 0.02092\, u(k-1)- 0.007459\, u(k-2)+1.822\, v_o(k-1)-0.8277\, v_o(k-2) \quad (18)$$

Figs. 7-a, b, c, d. show the numerical simulation results of the closed-loop digital PID voltage control system with desired voltage step is equal to 1.5V for the CPU in the smartphone. Based on off-line PSO algorithm parameters, after finishing 50 iterations, the best control gains parameters are obtained as kp=15.5796, ki=3.2035 and kd=0.8358. In Fig. 7-a. the output voltage response of the buck converter system was very small over-shoot in the transient state while the error voltage at steady state was equal to zero. In Fig. 7-b. the voltage error signal of the closed-loop buck converter controller system was a small value in the transient and it has become zero at the steady state. In Fig. 7-c. the action response of the digital PID controller was smooth without oscillation response, no spikes behavior and the action did not reach to the saturation state of 3.7 volt depending on the supply voltage. Fig. 7-d. clearly shows the improved performance index of the buck converter system related with the MSE for the off-line tuning PSO control methodology.

(a)



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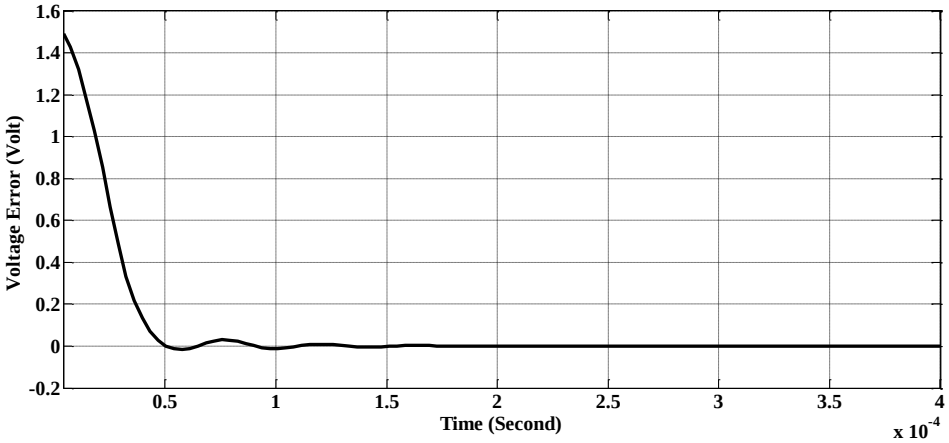
(b)



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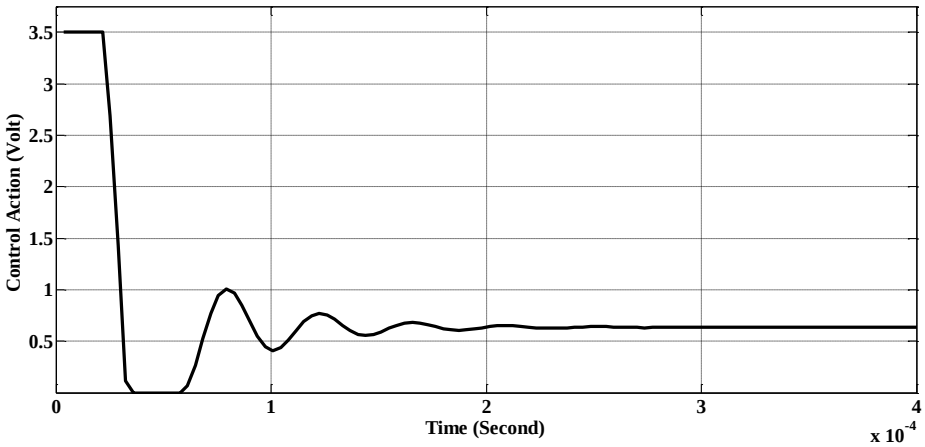

(d)

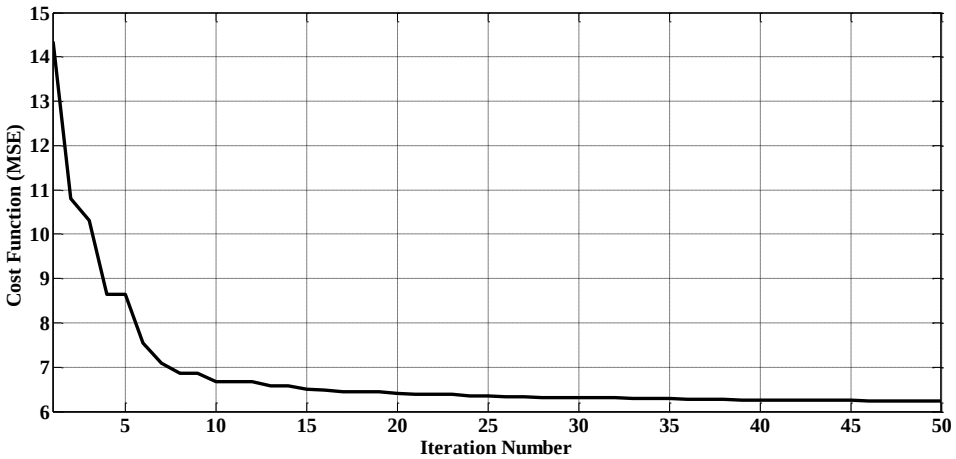

FIG. 7. THE DIGITAL SISO-PID CONTROLLER NUMERICAL SIMULATION RESULTS: (A) BUCK CONVERTER ACTUAL AND DESIRED OUTPUT VOLTAGE; (B) SIGNAL ERROR; (C) SIGNAL CONTROL OPERATION; (D) OFF-LINE PERFORMANCE INDEX (MSE).

The results of the proposed controller are compared with other types of controller results such as [18]; [2]; [20] as shown in Table 4.

TABLE 4. COMPARISON BETWEEN DIFFERENT TYPES OF CONTROLLER.

Type of controller	Over shoots	Steady-State Error	No. of Iterations	No. of Weights
MENN-PID [18]	2.3%	0.0	250 off-line	4
PID [2]	2.5%	0.0	600 on-line	3
Fuzzy-like PID [20]	4.8%	Small Oscillation	non	47 Fuzzy rules
Proposed Controller	1.8%	0.0	50 off-line	3

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Case II

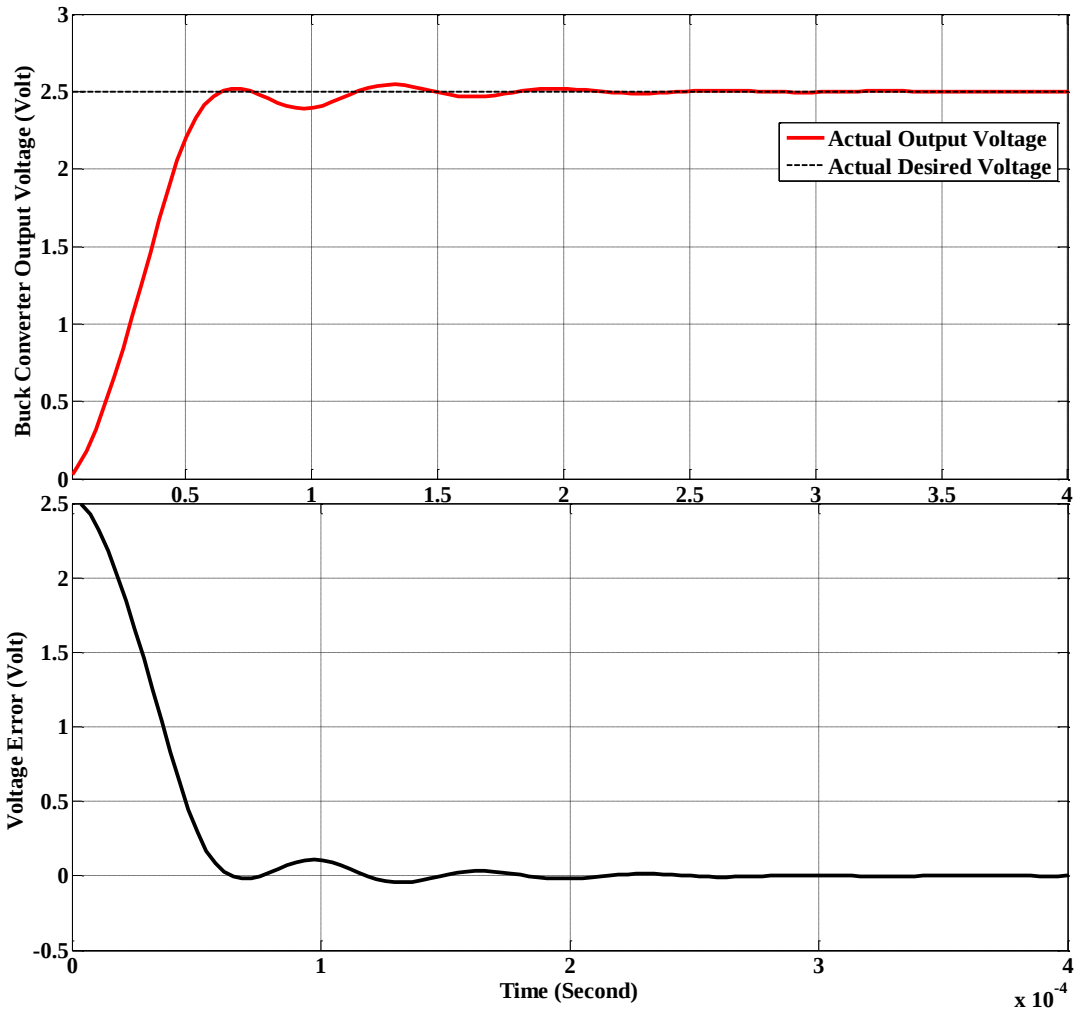
The difference equation of buck converter model for Wi-Fi application can be represented as in (19).

$$v_o(k) = 0.02098\, u(k-1) - 0.007481\, u(k-2) + 1.824\, v_o(k-1) - 0.8293\, v_o(k-2) \quad (19)$$

Figs. 8-a, b, c, d. show that the numerical simulation results of the closed-loop digital PID voltage control system with desired voltage step is equal to 2.5V in order to tune on Wi-Fi application in the smartphone. Based on off-line PSO algorithm parameters, after finishing 50 iterations, the best control gains parameters are obtained as kp=8.6038, ki=1.6646 and kd=1.0662. In Fig. 8-a. the output voltage response of the buck converter system was very small over-shoot in the transient state while the error voltage at steady state was equal to zero. In Fig. 8-b., the voltage error signal of the closed-loop buck converter controller system was a small value in the transient and it has become zero at the steady state. In Fig. 8-c., the action response of the digital PID controller was smooth without oscillation response, no spikes behavior and the action did not reach to the saturation state of 3.7 volt depending on the supply voltage. Fig. 8-d. clearly shows the improved performance index of the buck converter system related with the MSE for the off-line tuning PSO control methodology.

(a)

(b)



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(c)

(d)

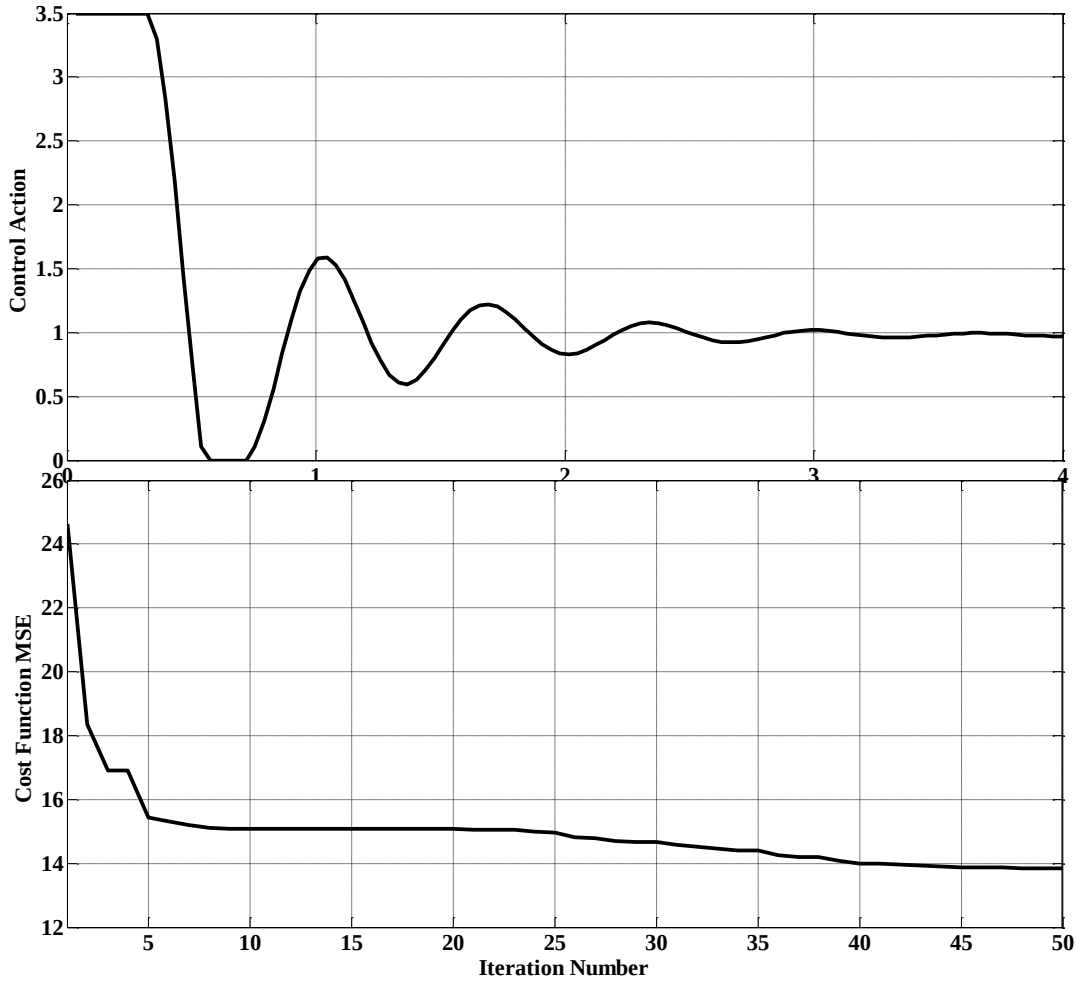

FIG. 8. THE DIGITAL SISO-PID CONTROLLER NUMERICAL SIMULATION RESULTS WHEN WI-FI APPLICATION TURN ON (A) BUCK CONVERTER ACTUAL AND DESIRED OUTPUT VOLTAGE ; (B) SIGNAL ERROR; (C) SIGNAL CONTROL OPERATION; (D) OFF-LINE PERFORMANCE INDEX (MSE).

Case III

To investigate the proposed SISO-PID controller has high robustness performance during load current variation by using many applications in the same time. BT application turns on at (0.403msec) in the smartphone in addition Wi-Fi application was turned on. Based on off-line PSO algorithm parameters, after finishing 50 iterations the best control gains parameters are obtained as kp=12.9689, ki=3.0456 and kd=2.4846.

As shown in Fig. 9-a. the output voltage response of the Buck converter system at (0.445 msec) was very small over-shoot and very small oscillation but the error voltage at steady-state was equal to zero.

In Fig. 9-b. the error voltage level between the actual and desired output voltage of the buck converter system at transient and steady states is small value, the error voltage became very nearby to zero and very small oscillation.

Fig. 9-c. illustrates the response of the control operation which has a fast and powerful adaptability with high performance of robustness because the control parameters are learned off-line PSO algorithm especially when turning on BT application (adding boundary disturbance) to show that the control operation has an ability to track the error signal of the buck converter system in order to follow the reference voltage as step change and minimize the disturbance effect of the load resistance.

Fig. 9-d. shows that the cost function of the off-line tuning PSO control algorithm is distinctly enhanced the behavior and performance of the proposed digital PID controller for the buck converter system

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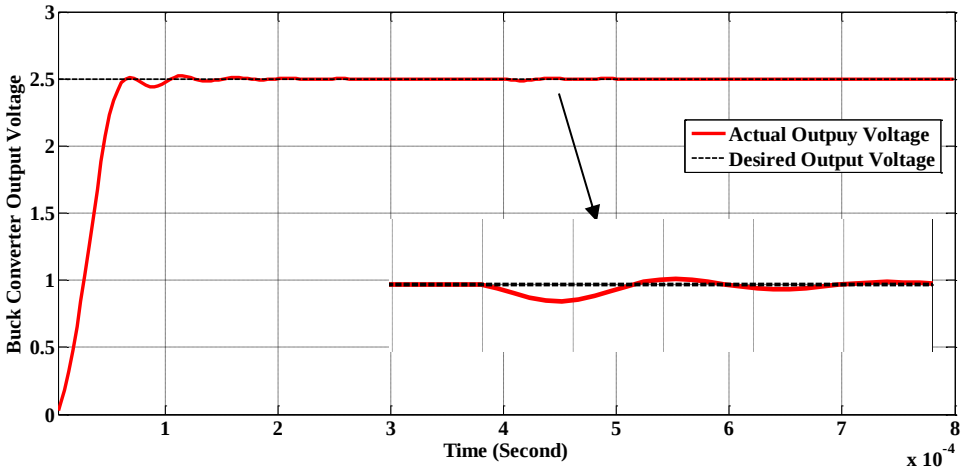
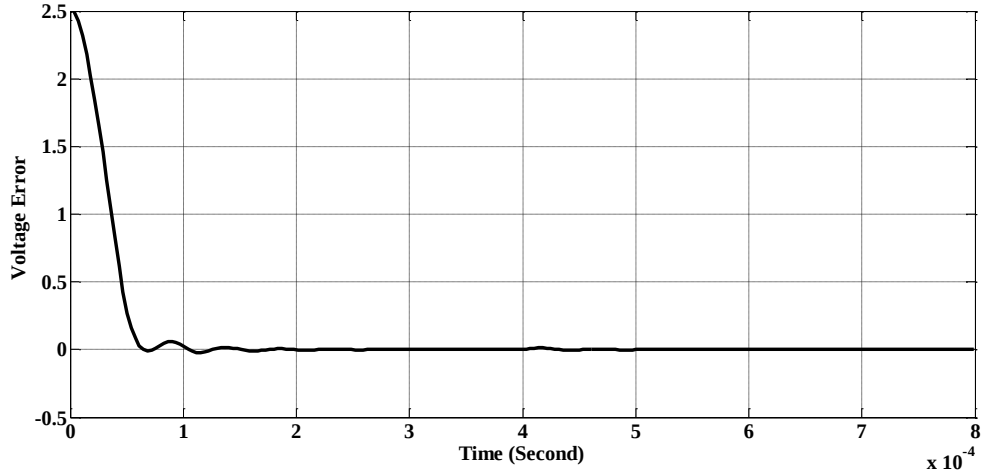
especially at time(0.4msec) during adding disturbance (turn on BT application) then difference equation of buck converter model for BT applications can be represented in (20).

$$v_o(k) = 0.02087\, u(k-1) - 0.007441\, u(k-2) + 1.82\, v_o(k-1) - 0.8263\, v_o(k-2) \quad (20)$$

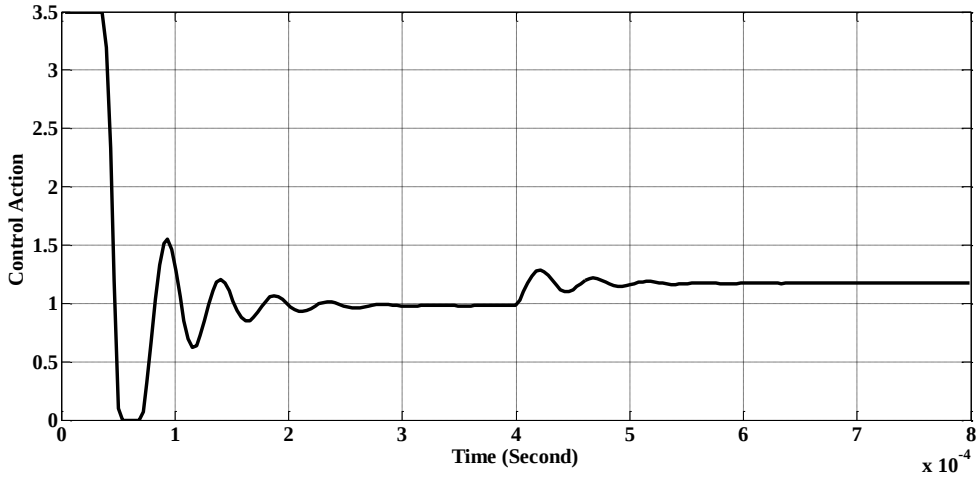
(a)



(b)



(c)



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(d)

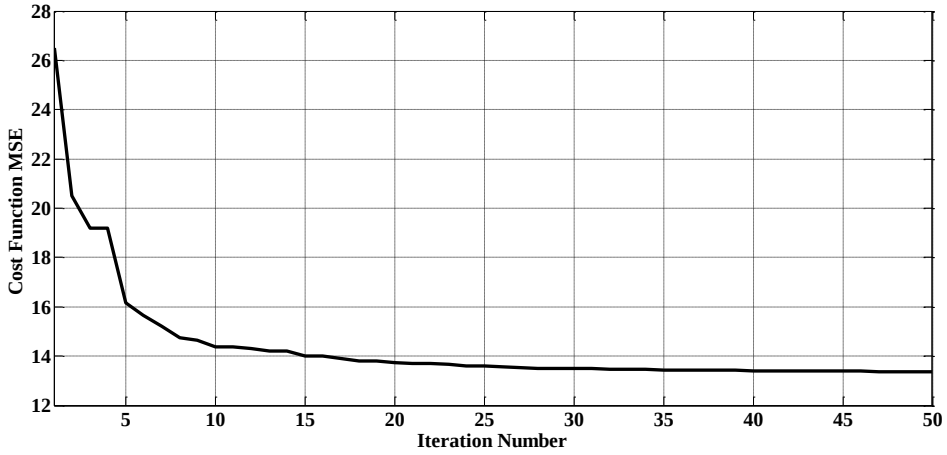

FIG. 9. THE DIGITAL SISO-PID CONTROLLER NUMERICAL SIMULATION RESULTS WHEN WI-FI+BT APPLICATION TURN ON (A) BUCK CONVERTER ACTUAL AND DESIRED OUTPUT VOLTAGE ; (B) SIGNAL ERROR; (C) SIGNAL CONTROL OPERATION; (D) OFF-LINE PERFORMANCE INDEX (MSE).

V. EXPERIMENTAL WORK

To carry out the proposed off-line SISO-FPGA-PID Verilog program controller, as shown in Fig. 3. MATLAB environment system uses the real-time Spartan-3E Starter kit with device xc3s500e-4fg320 as shown in Fig. 10.

FIG. 10. SPARTAN -3E STARTER KIT.

The proposed controller Verilog program file is extracted to the black box using the Xillinx-system generator in the MATLAB environment. The black box with the ports Gateway In and Gateway Out are shown in Fig. 11.

It is tested with the overall buck converter system under MATLAB environment before downloading as shown in Fig. 12.

This black box is utilized for downloading the bit-stream of the proposed SISO-FPGA-PID Verilog program controller on the Spartan-3E Starter Kit with the device xc3s500e-4fg320 through the system generator by using the Joint-Test-Action-Group (JTAG) as an interface and by the universal serial bus (USB) cable. The hardware co-simulation mechanism is utilized to implement this downloading process and to build the hardware of the designed controller. Firstly, the used kit name is selected from the HDL netlist. At the beginning of generating a co-simulation block, a finishing status was demonstrated. The XFlow is done without errors after finishing processes of generating, performing, synthesizing, and running. After finishing these processes successfully, a JTAG block is generated, as illustrated in Fig. 13.

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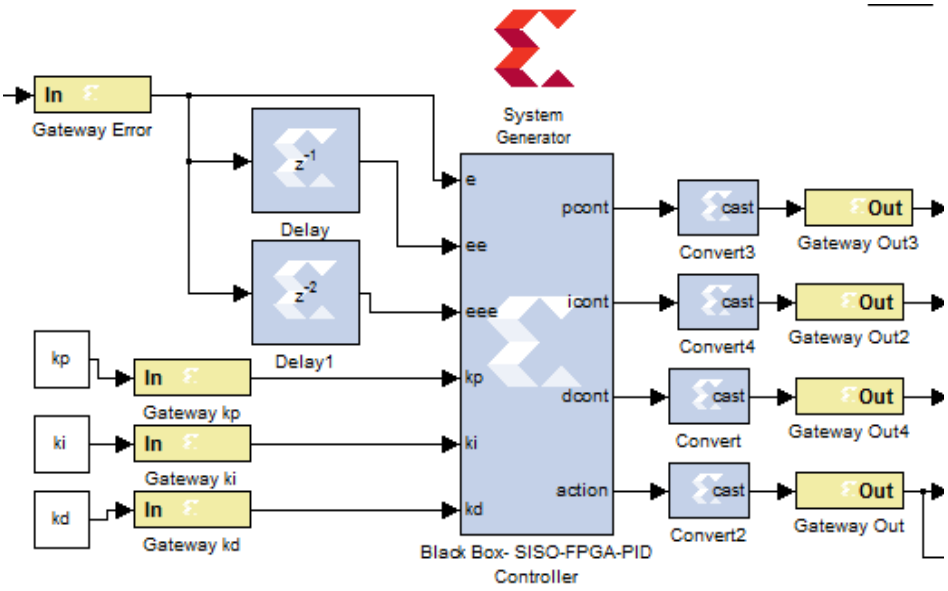

FIG. 11. THE BLACK BOX WITH THE GATEWAY IN AND GATEWAY OUT OF THE SISO-FPGA-PID CONTROLLER.

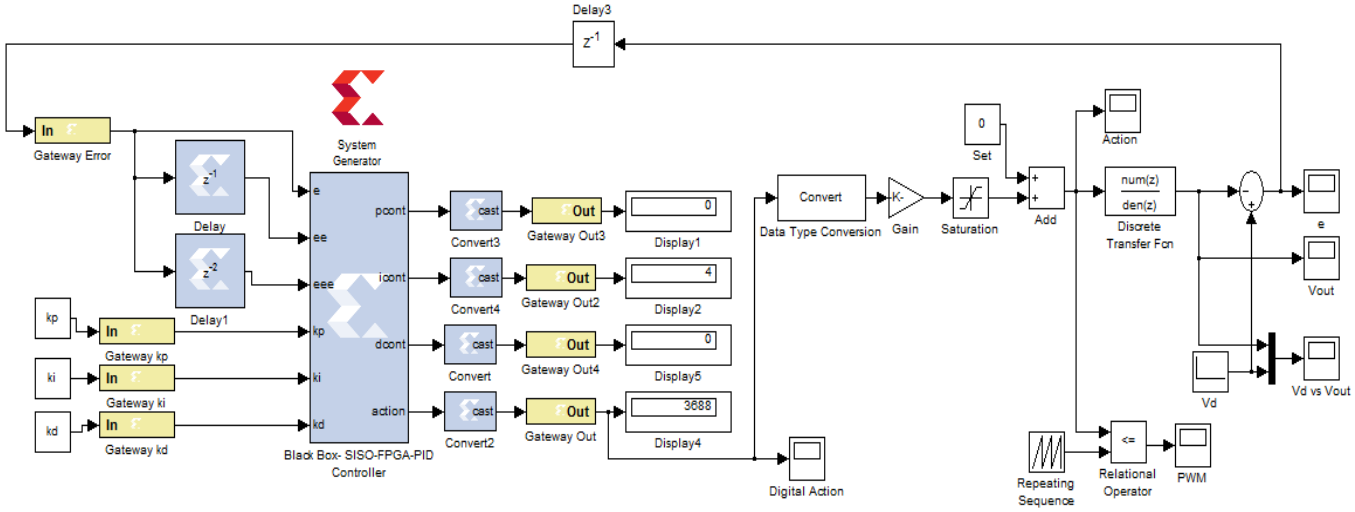

FIG. 12. THE OVERALL BUCK CONVERTER SYSTEM UNDER SISO-FPGA-PID CONTROLLER IN MATLAB ENVIRONMENT.

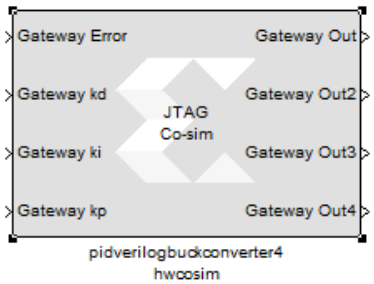

FIG. 13. JTAG BLOCK.

During the system simulation running, the interaction between the Spartan-3E Starter Kit and device xc3s500e-4fg320 by using the JTAG hwcosim (hardware co-simulation) interface block. The incoming data from the buck converter system is passed to the FPGA kit through the Gateway Ins, whereas the FPGA kit sends the control signal as output data to the buck converter system through the Gateway Out of the

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JTAG block. Hence, Figs. 14-a and b exhibit the block diagram of the proposed "SISO-FPGA-PID controller" for the buck converter system in the real-time.

In the real-time, Fig. 15-a. shows that the buck converter output voltage at transient state has a fast response with very small overshoots at desired voltage equal to 1.5 volt and the sampling time equal to 3.6 μsec and at steady-state the voltage error of the system is equal to zero. Fig. 15-b. illustrates the high performance of digital SISO-FPGA-PID controller in terms of fast generating digital voltage control action that it has the ability to track desired voltage of the buck converter model. The PWM signal is generated as in Fig. 15-c. and in Fig. 15-d. that show the error voltage level between the required and actual buck converter output voltage system which it has small value at transient then at steady states the error signal became very nearby to zero.

(a)

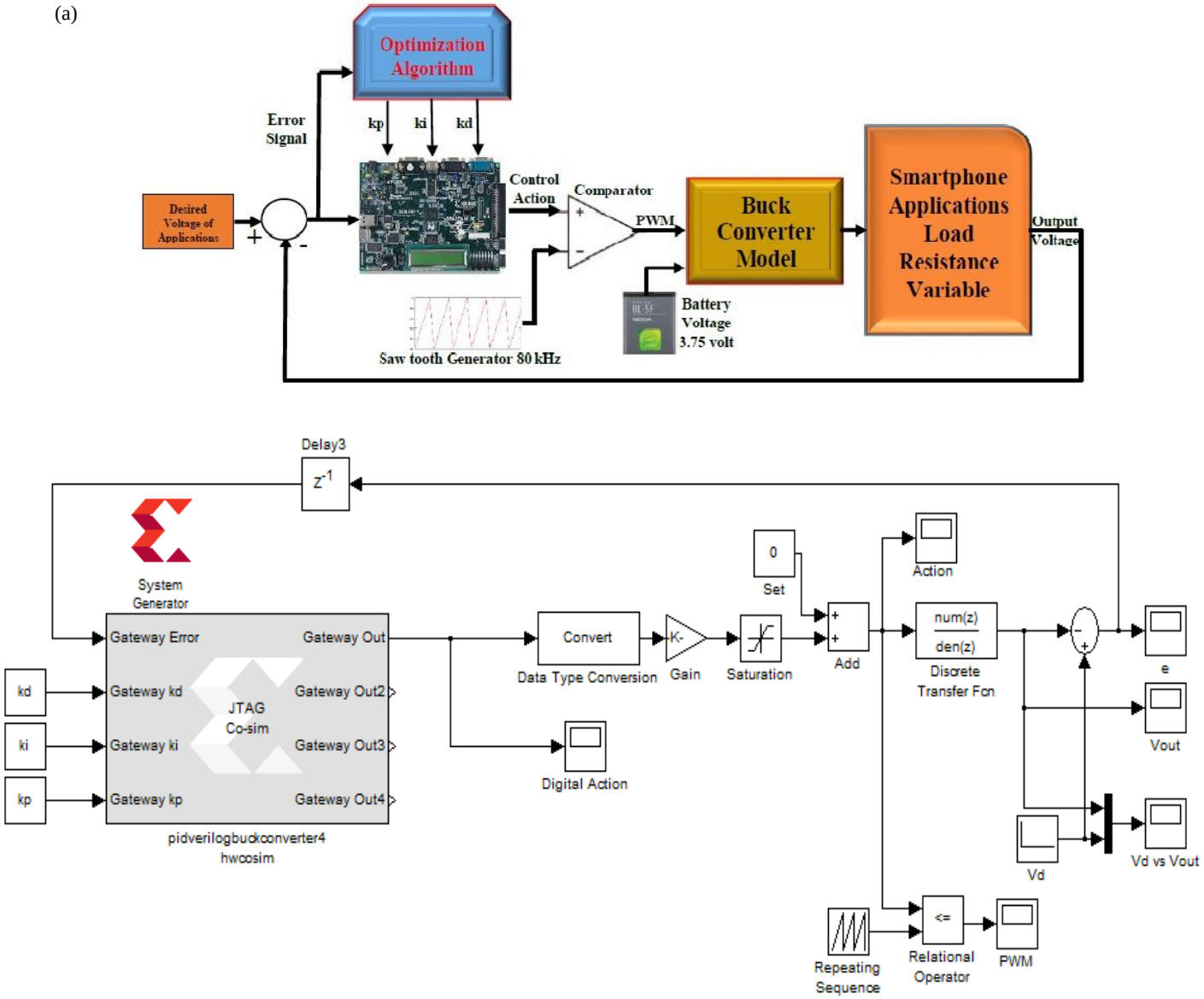

FIG. 14. (A) REAL-TIME PROPOSED SISO-FPGA-PID CONTROLLER BLOCK DIAGRAM; (B) SYSTEM GENERATOR IN THE MATLAB SIMULINK ENVIRONMENT.

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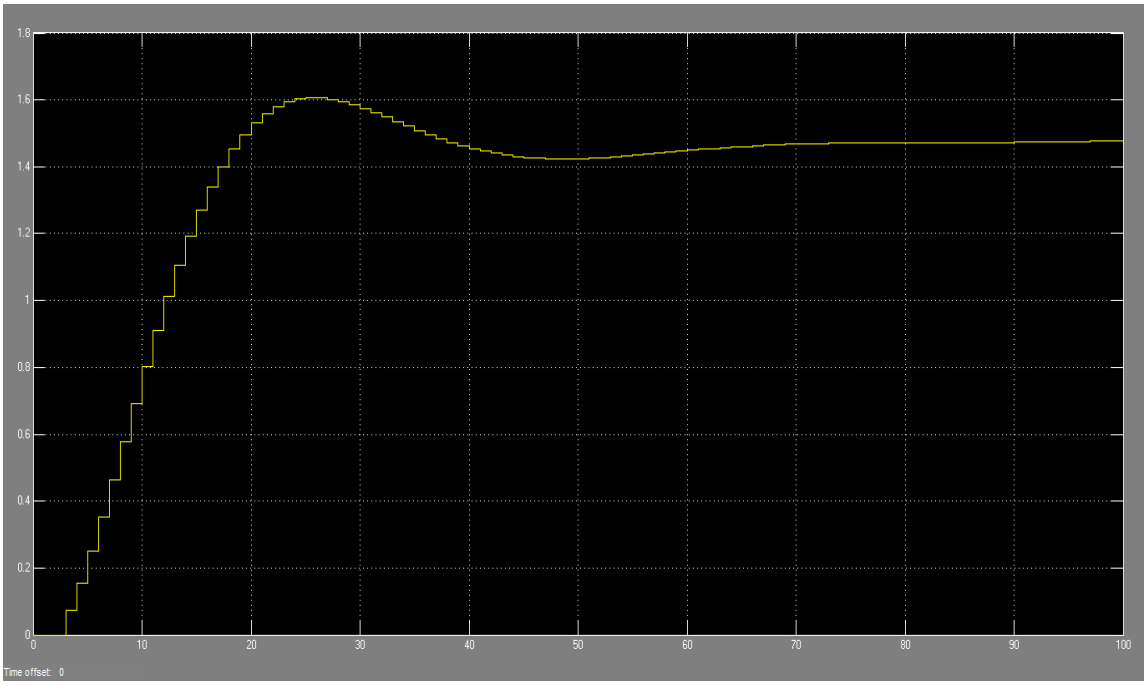
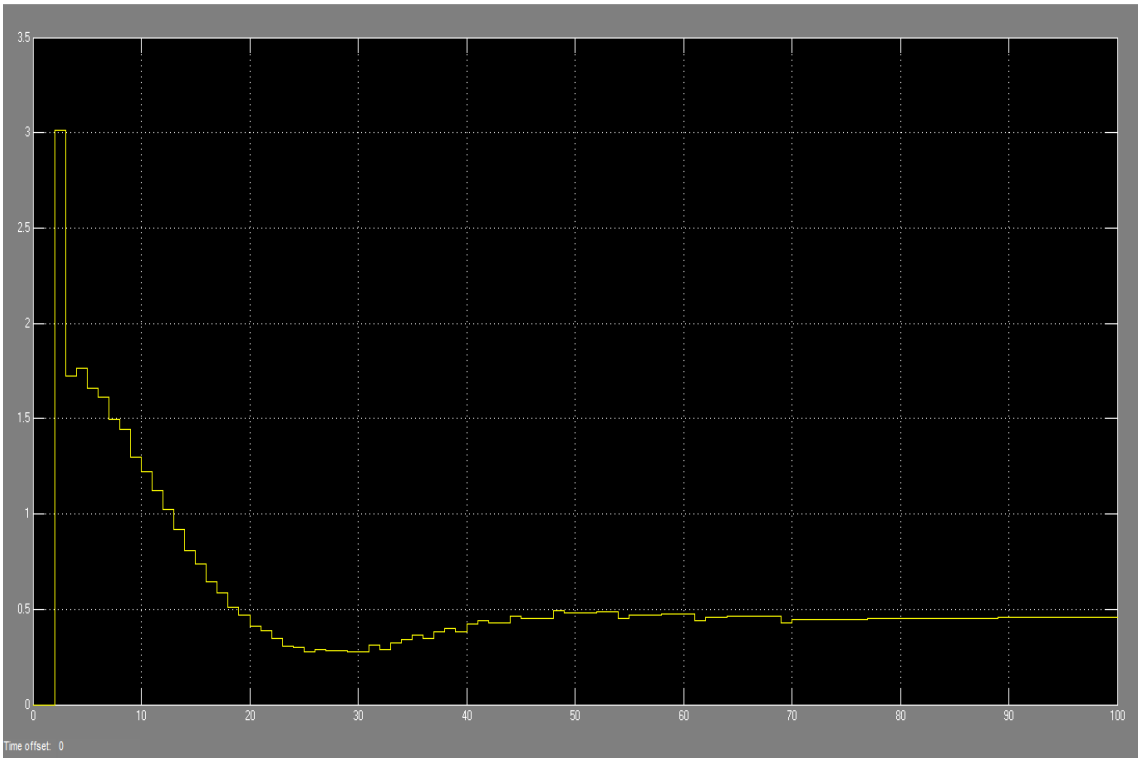


(a)



(b)

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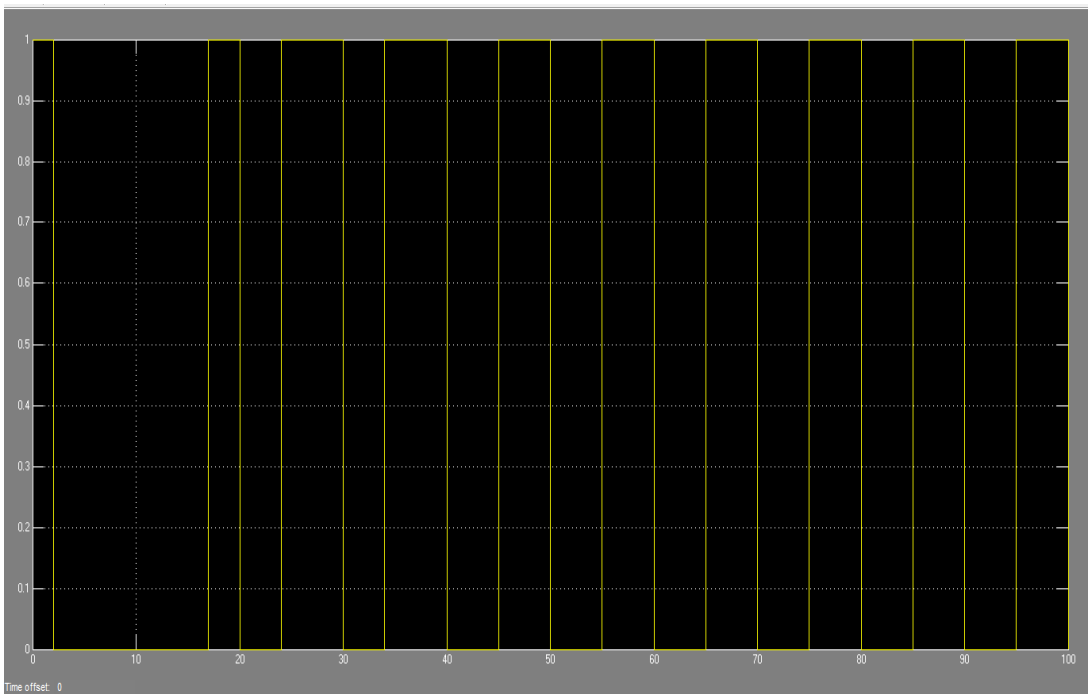
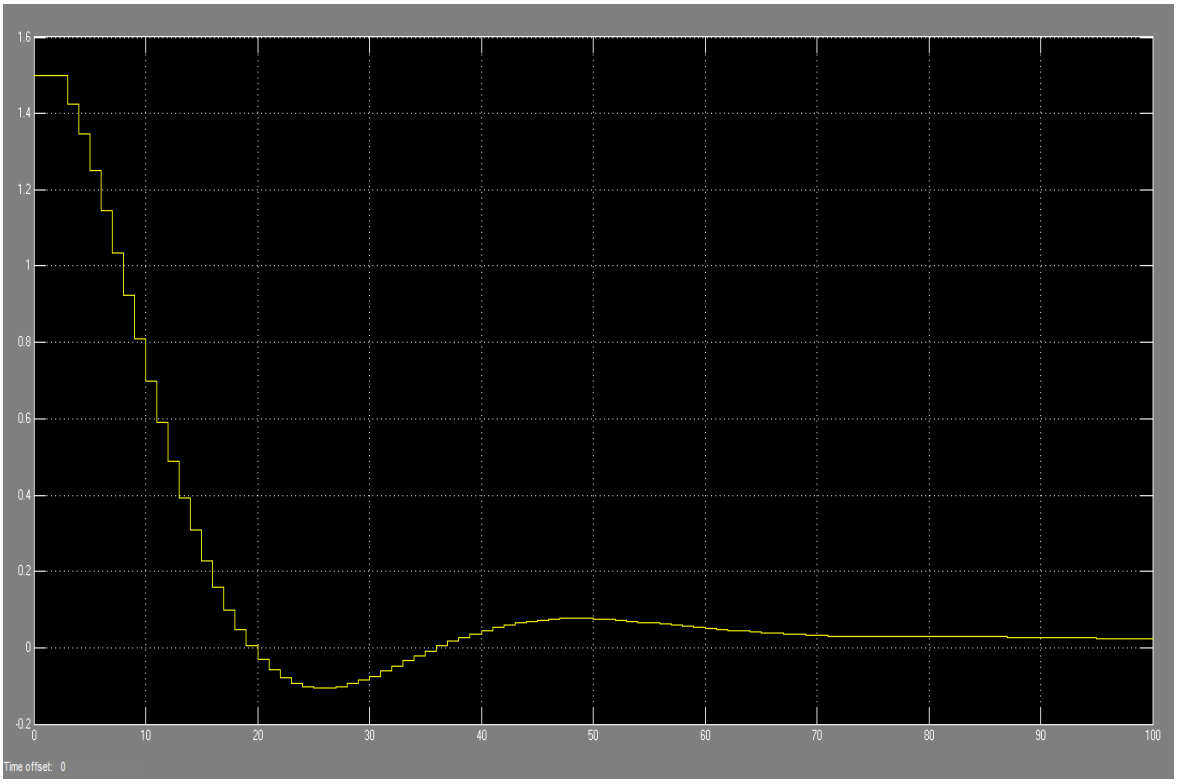


(c)



(d)

FIG. 15. THE REAL-TIME RESPONSE (A) BUCK CONVERTER ACTUAL OUTPUT VOLTAGE; (B) DIGITAL VOLTAGE CONTROL ACTION; (C) THE PWM SIGNAL; (D) THE ERROR VOLTAGE LEVEL.

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VI. CONCLUSIONS

This paper presents a proposed digital SISO-FPGA-PID controller with the off-line PSO algorithm that can be used to control the linear dynamic behaviour of a buck converter model in order to keep the voltage level delivered in each smartphone applications, and results of numerical MATLAB simulations and experimental Spartan-3E board work show that:

- The off-line PSO is a fast learning algorithm that can be used to generate voltage control action without an oscillation response or a saturation state problem.
- A minimum fitness evaluation is required to determine the optimal weight parameters for the "SISO-FPGA-PID controller".
- The strong robust SISO-FPGA-PID controller can track the output buck converter system to achieve the required voltage during using multi applications such as Wi-Fi, and BT at the same time.

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