_____

Exp. No. (6)

Flip – Flops

Object

1. To familiar the student with Flip-Flops.

2. To differentiate between various types of the Flip-Flops.

3. How to determine the next state of each type of Flip-Flops.

Theory

A Flip-Flop (F-F) is a multivibrator which has two stable state (Bistable) High and Low. Flip-Flop (F-F) are useful devices for applications such as counting, storing binary data and data conversion from serial to parallel

There are many different types of Flip-Flops:

1. a) Simple Set-Reset (S-R) Flip-Flip.

    b) Clocked (S-R) Flip-Flop.

2. J-K Flip-Flop.

3. D-Type Flip-Flop.

4. T-Type Flip-Flop.

1. a) *The Set-Rest (S-R) Flip-Flop:*

Fig. (1) shows the basic construction of S-R F-F. It has two output called Q and $\overline{Q}$ and like the toggle switch, when it's (1) output is high, it's (0) output is low and vice-versa.

When the power is applied to the machine the F-F will go either to it's (Set) or (Reset) state. The initial state is arbitrary depending on the relative characteristics of the components which comprise the two logic gates.

Fig. (1-b) shows the meaning of Set and Reset states in terms of binary voltage levels. To see how F-F operates, refer to Fig. (1-a), Assume that the initial state is the (Set) state (L_1 ON and L_2 OFF), and that both the Set and Reset lines are low (0). The Set and Reset lines are both stable when they are low. In the Set state gate N_1 provides a high level to upper inputs of the N_2. Therefore, both input to N_2 are high causing it to produce a low output which turns L_2 OFF. The low output of N_2 is also applied to the lower input terminal of N_1. This produces a high output from gate N_1, turning L_1 ON. In the set state then, N_2 is continually enabling N_1, and N_1 continually disabling N_2.

The two gates are latched in a condition that will remain until the input conditions on the S-R lines are changes.

If the F-F is initially in the Reset state (L_2 ON and L_1 OFF), in this case N_1 is continually enabling N_2 and N_2 is continually disabling N_1. The circuit is again latched output but in the opposite direction.

Apply a high to the S terminal with the F-F in the Reset state (L_2 ON and L_1 OFF) at this case the output N_1 go to High, reversing the latch condition of the previous case. If a high is then applied to the R terminal, the latch condition is reverses again (i.e. the L_1 is OFF and L_2 is ON).

The truth table for the S-R F-F is shown in Fig.(1-b). As the first line of the truth table shows no change (N.C.) occur in the F-F state if both S and R lines are Low (0).

The second line shows the input conditions needed to cause the F-F to go to the Reset state.

The third line of the truth table shows the input condition needed to cause the F-F to go to the Set State.

The fourth line shows a set of "illegal" input conditions which are usually avoided by the machine designer.

The F-F cannot "remember" this state. Since the primary value of the F-F is in its memory capability. The "illegal" input-output situation can be ignored.

1. b) *The Clocked Set-Rest (Clock S-R) Flip-Flop:*

It is also called Steered S-R Flip-Flop. When a F-F is used, it is frequently desirable to establish the desired Set or Rest state first, then have it go to that state at some later point in time.

The process of pre-establishing the desired state is called (Steering).

Fig.(2) shows a simple form of clocked S-R F-F. It is the same S-R F-F of Fig.(1-a) except that a steering network comprised of additional logic gates (N_3 and N_4) has been added to the input circuit. The input levels at steering terminals A and B cannot by themselves change the state of the F-F. A "trigger" or "clock" pulse or EXT. signal shot must be applied. When this occurs, the F-F will go to the state directed by the HIGH-LOW conditions at the steering terminal. If A is High when the clock pulse is applied, gate N_4 will be enabled. This provide a low level to N_2 switching the F-F to the reset state.

2. *The J-K Flip-Flop:*

The J-K F-F combines the capability of the S-R and clocked S-R Flip-Flops into a single element. Fig.(4-a) shows the combination of the J-K F-F, and Fig. (4-b) shows the truth table of the J-K F-F.

3. *D-Type Flip-Flop:*

A D-type Flip-Flop can constructed from the S-R F-F as shown in Fig. (3) and from J-K F-F as shown in Fig.(6).

4. *T-Type Flip-Flop:*

A T-type F-F can be constructed from the J-K F-F as shown in Fig. (7).

Procedure:

1. Hook up the simple S-R F-F circuit shown in Fig. (1-a) by using integrated circuit (I.C) type ------------ and state it's truth table.

   Note:

   Logic (1) = + 5 Volt = + VCC = HIGH.

   Logic (0) = 0 Volt   = GND   = LOW.

2. Hook up the steering circuit for the clock S-R F-F of Fig.(2) and determine the next state truth table when:

   a. Clock equal to zero (GND) (Logic 0).

   b. Clock equal to + VCC (Logic 1).

3. Hook up D-type F-F in Fig. (3) by using (I.C.), type --------------- with clock terminal set to EXT signal shot, when D in it's low position (GND). State the output Q, and when D in it's high position (+VCC) state the output Q.

4. Hook up J-K F-F shown in Fig.(5-a) and determine the output of the truth table of Fig. (5-b) by using (I.C.) type --------------------- .

5. Hook up the circuit shown in Fig. (6) D-type F-F by using (I.C.) type ---------------- and state it's truth table.

6. Repeat step 5 for Fig. (7) T-type F-F.

Discussion:

1. For the simple S-R F-F try to implement the same F-F using two NOR gates, give it's truth table.

2. What is the advantage of using J-K F-F over other types of Flip-Flops.

3. Give an electronic circuit using discrete components i.e. transistors. Diodes and resistors for J-K F-F.

4. From the clocked S-R F-F, show how can you form D-type and T-type Flip-Flops.
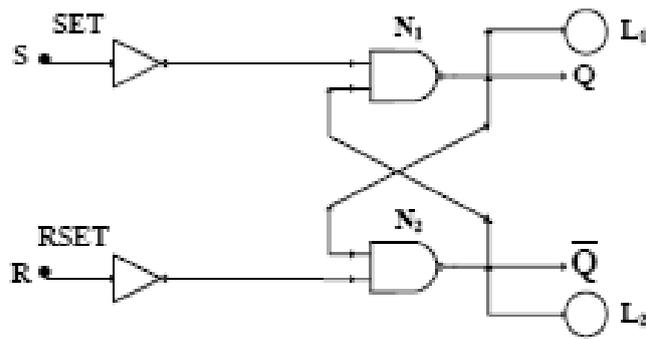
I/P		O/P	
S	R	Q	$\overline{Q}$
0	0	N.C	N.C
0	1	0	1
1	0	1	0
1	1	1	1

Fig. (1-a) S-R Flip-Flop Construction.   Fig. (1-b) Truth Table of S-R Flip-Flop .
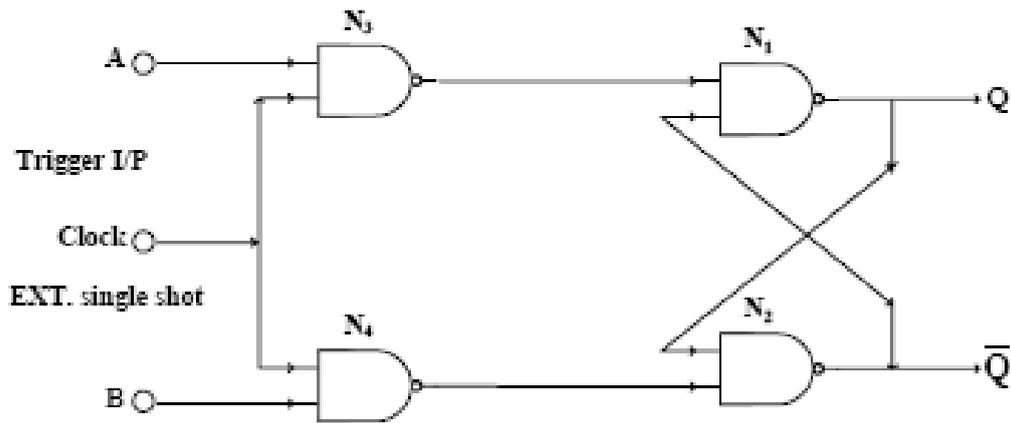
Fig. (2)
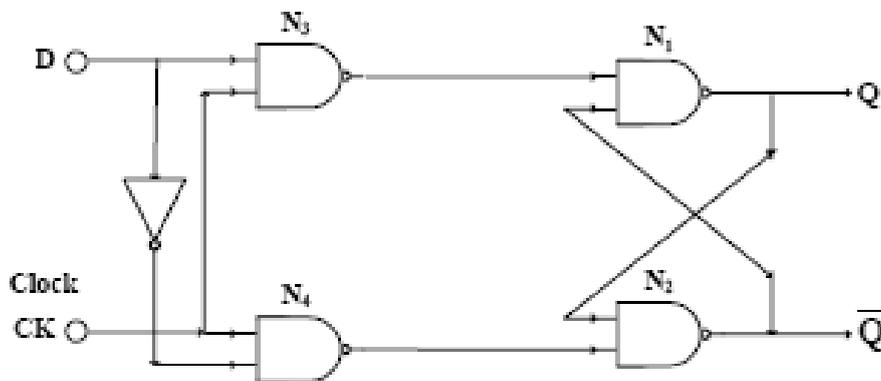Steering Circuit or Clocked S-R Flip-Flop.
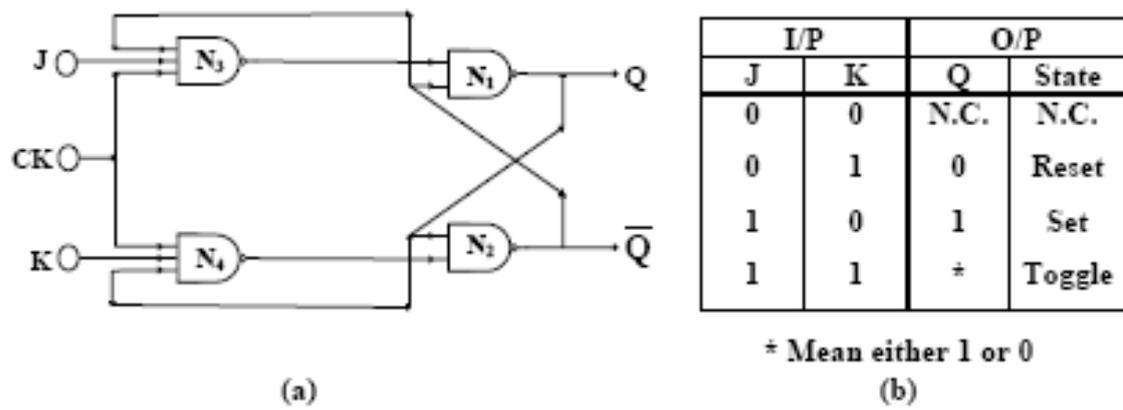

Fig. (3)
D-Type Flip-Flop Construction.

I/P		O/P	
J	K	Q	State
0	0	N.C.	N.C.
0	1	0	Reset
1	0	1	Set
1	1	*	Toggle

* Mean either 1 or 0

(a)   (b)

Fig. (4)
(a): J-K F-F Construction. / (b): J-K F-F Truth Table.

I/P Before Clock					O/P After Clock	
S	R	J	K	Q	Q(n+1)	State
1	1	0	0	0		
1	1	0	0	1		
1	1	0	1	0		
1	1	0	1	1		
1	1	1	0	0		
1	1	1	0	1		
1	1	1	1	0		
1	1	1	1	1		

(a)   (b)
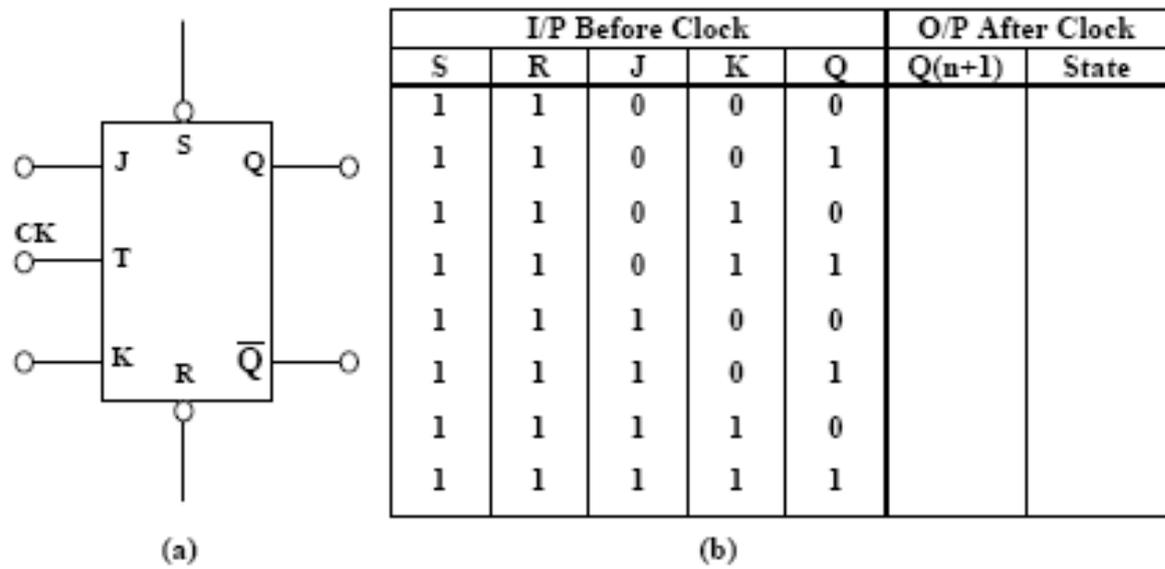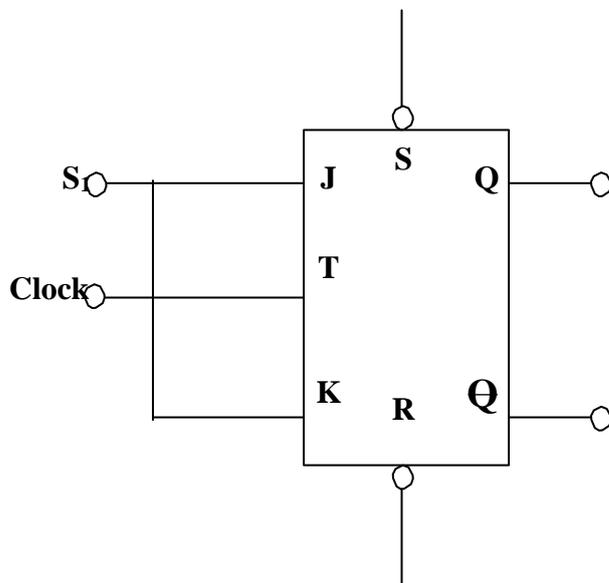
Fig. (5)
(a): J-K F-F Chip. / (b): J-K F-F Truth Table.

38
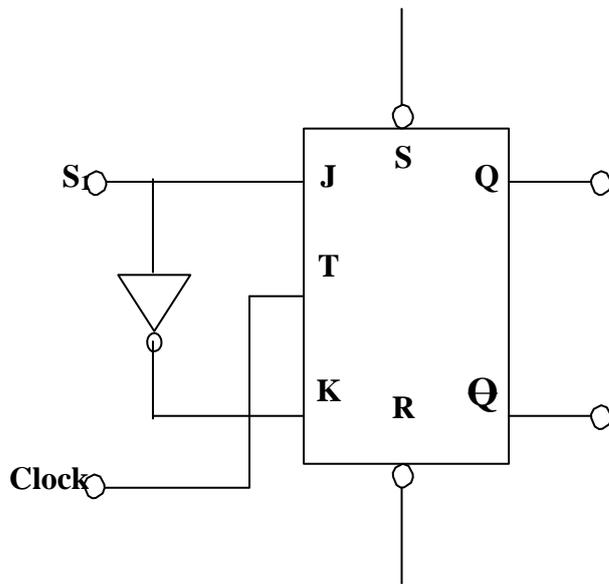
Fig. (6)
D-Type Flip-
Flop

Fig. (7)
T-Type Flip-
Flop