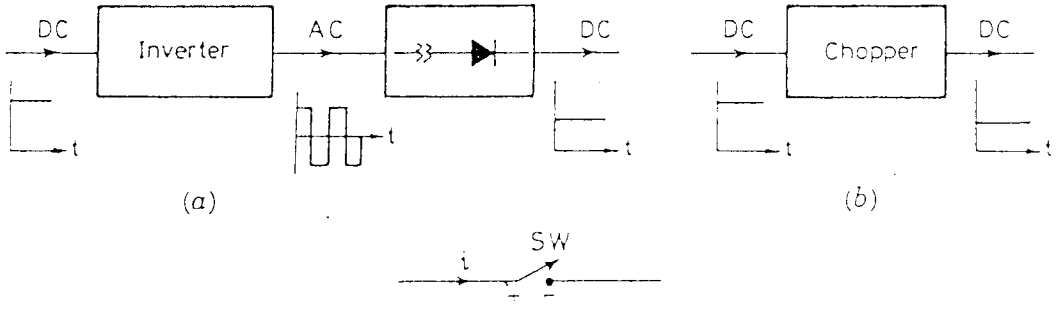
SEVEN

Choppers

Many industrial applications require power from dc voltage sources. Several of these applications, however, perform better in case these are fed from variable dc voltage sources. Examples of such dc systems are subway cars, trolley buses, battery-operated vehicles, battery-charging etc.

From ac supply systems, variable dc output voltage can be obtained through the use of phase-controlled converters (discussed in Chapter 6) or motor-generator sets. The conversion of fixed dc voltage to an adjustable dc output voltage, through the use of semiconductor devices, can be carried out by the use of two types of dc to dc converters given below [5].

AC Link Chopper. In the ac link chopper, dc is first converted to ac by an inverter (dc to ac converter). AC is then stepped-up or stepped-down by a transformer which is then converted back to dc by a diode rectifier Fig. 7.1 (*a*). As the conversion is in two stages, dc to ac and then ac to dc, ac link chopper is costly, bulky and less efficient.



(*a*) AC link chopper (*b*) dc chopper (or chopper) and
(*c*) Reproduction of a power semiconductor device.
Fig. 7.1

DC Chopper. A chopper is a static device that converts fixed dc input voltage to a variable output voltage directly Fig. 7.1 (*b*). A chopper may be thought of as dc equivalent of an ac transformer since they behave in an identical manner. As choppers involve one stage conversion, these are more efficient

Choppers are now being used all over the world for rapid transit systems. These are also used in trolley cars, marine hoists, forklift trucks and mine haulers. The future electric automobiles are likely to use choppers for their speed control and braking. Chopper systems offer smooth control, high efficiency, fast response and regeneration.

The power semiconductor devices used for a chopper circuit can be power BJT, power MOSFET, GTO or force-commutated thyristor. These devices, in general, can be represented by a switch SW with an arrow as shown in Fig. 7.1 (*c*). When the switch is off no current can flow. When the switch is on, current flows in the direction of arrow only. The power semiconductor devices have on-state voltage drops of 0.5 V to 2.5 V across them. For the sake of simplicity, this voltage drop across these devices is neglected.

As stated above, a chopper is dc equivalent to an ac transformer having continuously variable turns ratio. Like a transformer, a chopper can be used to step down or step up the fixed dc input voltage. As step-down dc choppers are more common, a dc chopper in this book would mean a step-down dc chopper unless stated otherwise.

The object of this chapter is to discuss the basic principles of chopper operation and the more common types of chopper configurations using ideal switches.

7.1. PRINCIPLE OF CHOPPER OPERATION

A chopper is a high speed on/off semiconductor switch. It connects source to load and disconnects the load from source at a fast speed. In this manner, a chopped load voltage as shown in Fig. 7.2 (*b*) is obtained from a constant dc supply of magnitude V_s. In Fig. 7.2 (*a*), chopper is represented by a switch *SW* inside a dotted rectangle, which may be turned-on or turned-off as desired. For the sake of highlighting the principle of choper operation, the circuitry used for controlled the on, off periods of this switch is not shown. During the period

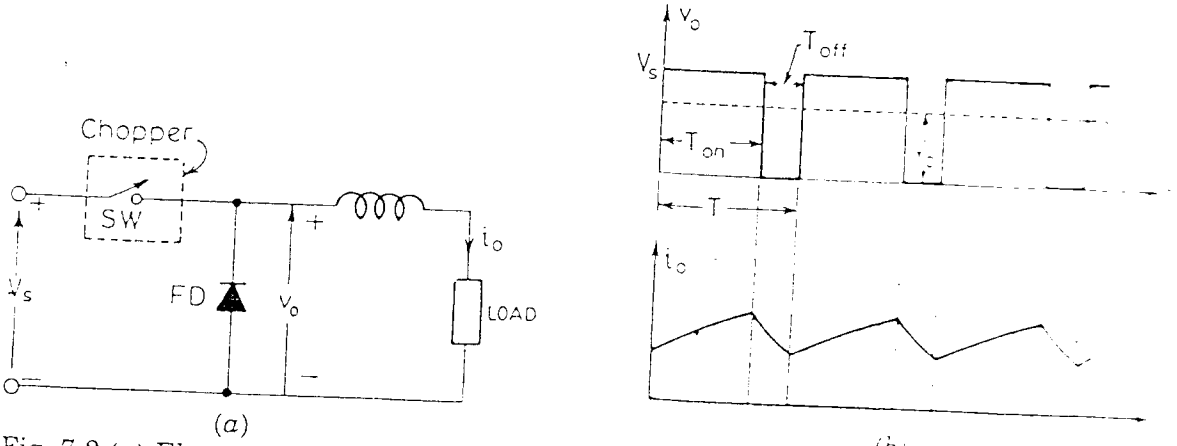


Fig. 7.2 (*a*) Elementry chopper circuit and (*b*) output voltage and current waveforms

T_{on}, chopper is on and load voltage is equal to source voltage V_s. During the interval T_{off} chopper is off, load current flows through the freewheeling diode *FD*. As a result load terminals are short circuited by *FD* and load voltage is therefore zero during T_{off}. In this manner, a chopped dc voltage is produced at the load terminals. The load current as shown in Fig. 7.2 (*b*) is continuous. From Fig. 7.2 (*b*), average load voltage V_0 is given by

$$V_0 = \frac{T_{on}}{T_{on} + T_{off}} V_s = \frac{T_{on}}{T} V_s = \alpha V_s \qquad \ldots (7.1)$$

where

T_{on} = on-time ; T_{off} = off-time

$T = T_{on} + T_{off}$ = chopping period

$\alpha = \dfrac{T_{on}}{T}$ = duty cycle

Thus load voltage can be controlled by varying duty cycle α. Eq. (7.1) shows that dc voltage is independent of load current. Eq. (7.1) can also be written as

$$V_0 = f \cdot T_{on} \cdot V_s \qquad ...(7.2)$$

where $f = \frac{1}{T}$ = chopping frequency

7.2. CONTROL STRATEGIES

It is seen from Eq. (7.1) that average value of output voltage V_0 can be controlled through α by opening and closing the semiconductor switch periodically. The various control strategies for varying duty cycle α are as follows :

7.2.1. Constant Frequency System

In this scheme, the on-time T_{on} is varied but chopping frequency f (or chopping period T) is kept constant. Variation of T_{on} means adjustment of pulse width, as such this scheme is also called *pulse-width-modulation scheme*. This scheme has also been referred to as *time-ratio control* (TRC) by some authors.

Fig. 7.3 illustrates the principle of pulse-width modulation. Here chopping period T is constant. In Fig. 7.3 (*a*), $T_{on} = \frac{1}{4} T$ so that $\alpha = 0.25$ or $\alpha = 25\%$. In Fig. 7.3 (*b*), $T_{on} = \frac{3}{4} T$ so that $\alpha = 0.75$ or 75%. Ideally α can be varied from zero to infinity. Therefore output voltage V_0 can be varied between zero and source voltage V_s.

7.2.2. Variable Frequency System

In this scheme, the chopping frequency f (or chopping period T) is varied and either (*i*) on-time T_{on} is kept constant or (*ii*) off-time T_{off} is kept constant. This method of controlling α is also called frequency-modulation scheme.

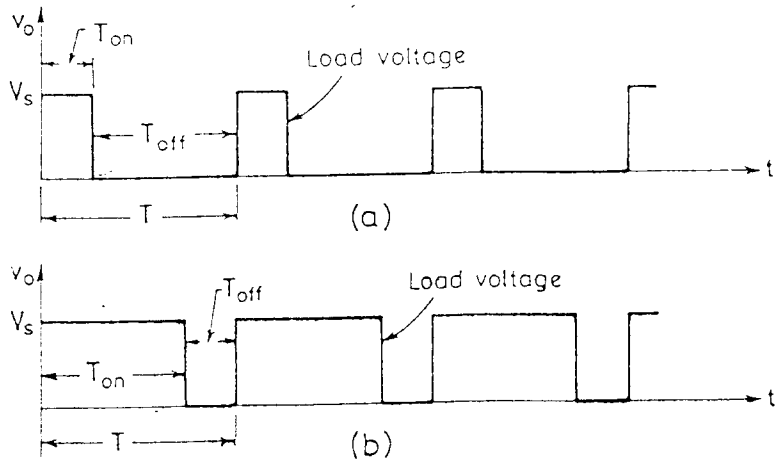


Fig. 7.3. Principle of pulse-width modulation (constant T).

Fig. 7.4 illustrates the principle of frequency modulation. In Fig. 7.4 (*a*), T_{on} is kept constant but T is varied. In the upper diagram of Fig. 7.4 (*a*), $T_{on} = \frac{1}{4} T$ so that $\alpha = 0.25$. In the lower diagram of Fig. 7.4 (*a*), $T_{on} = \frac{3}{4} T$ so that $\alpha = 0.75$. In Fig. 7.4 (*b*), T_{off} is kept constant and T is varied. In the upper diagram of this figure, $T_{on} = \frac{1}{4} T$ so that $\alpha = 0.25$ and in the lower diagram $T_{on} = \frac{3}{4} T$ so that $\alpha = 0.75$.

Frequency modulation scheme has some disadvantages as compared to pulse-width modulation scheme. These are as under :

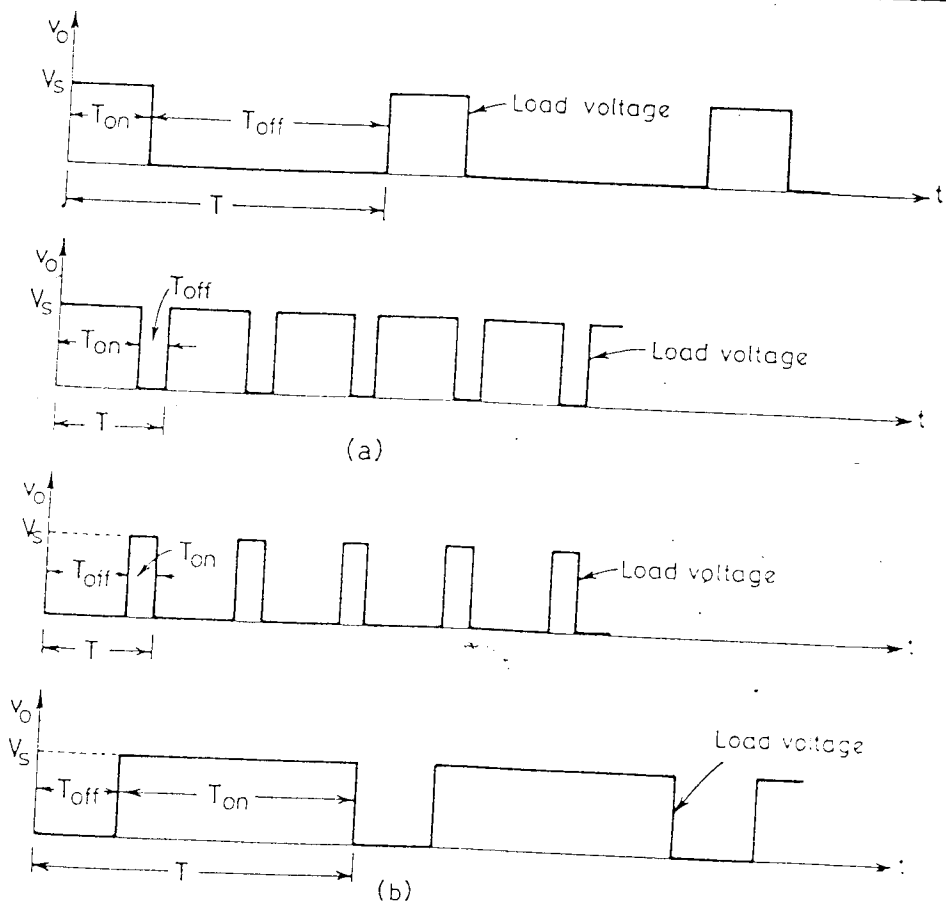


Fig. 7.4. Principle of frequency modulation.
(*a*) on-time T_{on} constant and (*b*) off-time T_{off} constant.

(*i*) The chopping frequency has to be varied over a wide range for the control of output voltage in frequency modulation. Filter design for such wide frequency variation is, therefore quite difficult.

(*ii*) For the control of α, frequency variation would be wide. As such, there is a possibility of interference with signalling and telephone lines in frequency modulation scheme.

(*iii*) The large off-time in frequency modulation scheme may make the load current discontinuous which is undesirable.

It is seen from above that constant frequency (*PWM*) scheme is better than variable frequency scheme. *PWM* technique has, however, a limitation. In this technique, T_{on} cannot be reduced to near zero for most of the commutation circuits used in choppers. As such, the range of α control is not possible in *PWM*. This can, however, be achieved by increasing the chopping period (or decreasing the copping frequency) of the chopper.

7.3. STEP-UP CHOPPERS

For the chopper configuration of Fig. 7.2 (*a*), average output voltage V_0 is less than the input voltage V_s, *i.e.* $V_0 < V_s$; this configuration is therefore called step-down chopper. Average output voltage V_0 greater than input voltage V_s can, however, be obtained by a chopper called *step-up chopper*. Fig. 7.5 (*a*) illustrates an elementary form of a step-up chopper. In this article working principle of a step-up chopper is presented.

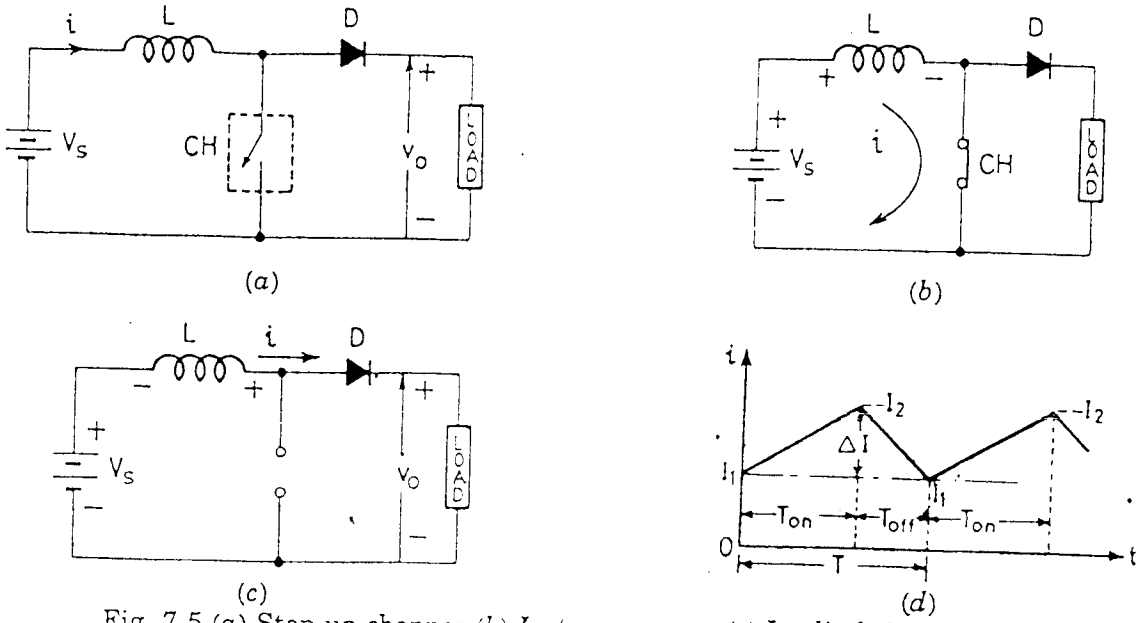


Fig. 7.5 (*a*) Step-up chopper (*b*) L stores energy (*c*) $L \cdot di/dt$ is added to V_s (*d*) current waveform.

In this chopper, a large inductor L in series with source voltage V_s is essential as shown in Fig. 7.5 (*a*). When the chopper CH is on, the closed current path is as shown in Fig. 7.5 (*b*) and inductor stores energy during T_{on} period. When the chopper CH is off, as the inductor current cannot die down instantaneously, this current is forced to flow through the diode and load for a time T_{off}, Fig. 7.5 (*c*). As the current tends to decrease, polarity of the emf induced in L is reversed as shown in Fig. 7.5 (*c*). As a result, voltage across the load, given by $V_0 = V_s + L\,(di/dt)$, exceeds the source voltage V_s. In this manner, the circuit of Fig. 7.5 (*a*) acts as a step-up chopper and the energy stored in L is released to the load.

When CH is on, current through the load would increase from I_1 to I_2 as shown in Fig. 7.5 (*d*). When CH is off, current would fall from I_2 to I_1. With CH on, source voltage is applied to L *i.e.* $v_L = V_s$. When CH is off, KCL for Fig. 7.5 (*c*) gives $v_L - V_0 + V_s = 0$, or $v_L = V_0 - V_s$. Here v_L = voltage across L. Assuming linear variation of output current, the energy input to inductor from the source, during the period T_{on}, is

$$W_{in} = (\text{voltage across } L)\,(\text{average current through } L)\,T_{on}$$

$$= V_s \cdot \left(\frac{I_1 + I_2}{2}\right) T_{on} \qquad \ldots(7.3)$$

During the time T_{off}, when chopper is off, the energy released by inductor to the load is

$$W_{off} = (\text{voltage across } L)\,(\text{average current through } L)\,T_{off}$$

$$= (V_0 - V_s)\left(\frac{I_1 + I_2}{2}\right) \cdot T_{off} \qquad \ldots(7.4)$$

Considering the system to be lossless, these two energies given by Eqs. (7.3) and (7.4) will be equal.

$$\therefore \quad V_s \left(\frac{I_1 + I_2}{2}\right) T_{on} = (V_0 - V_s)\left(\frac{I_1 + I_2}{2}\right) \cdot T_{off}$$

or

$$V_0 = V_s \frac{T}{T - T_{on}} = V_s \frac{1}{1 - \alpha} \qquad \ldots(7.5)$$

It is seen from Eqn. (7.5) that average voltage across the load can be stepped up by var the duty cycle. If chopper of Fig. 7.5 (*a*) is always off, $\alpha = 0$ and $V_0 = V_s$. If this chopp always on, $\alpha = 1$ and $V_0 = \infty$ (infinity). In practice, chopper is turned on and off s that variable and the required step-up average output voltage, more than source voltag obtained.

The principle of step-up chopper can be employed for the regenerative braking c motors. In Fig. 7.5 (*a*), if V_s represents the motor armature voltage and V_0 the dc so voltage, the power can be fed back to the dc source in case $V_s/(1-\alpha)$ is more than V_0. In manner, regenerative braking of dc motor occurs. Even at decreasing motor spe regenerative braking can be made to take place provided duty cycle α is so adjusted $V_s/(1-\alpha)$ exceeds the fixed source voltage V_0.

Example 7.1 *For the basic dc to dc converter of Fig. 7.2 (a), express the following varia as functions of V_s, R and duty cycle α in case load is resistive :*

(a) Average output voltage and current
(b) Output current at the instant of commutation
(c) Average and rms freewheeling diode currents
(d) Rms value of the output voltage
(e) Rms and average thyristor currents
(f) Effective input resistance of the chopper.

Solution. The load voltage variation is shown in Fig. 7.2 (*b*). For a resistive load, ou or load current waveform is similar to load voltage waveform.

(*a*) Average output voltage, $V_0 = \dfrac{T_{on}}{T} V_s = \alpha V_s$

Average output current, $I_0 = \dfrac{V_0}{R} = \dfrac{T_{on}}{T} \cdot \dfrac{V_s}{R} = \alpha \dfrac{V_s}{R}$

(*b*) The output current is commutated by the thyristor at the instant $t = T_{on}$. There output current at the instant of commutation is V_s/R.

(*c*) For a resistive load, freewheeling diode FD does not come into play. Therefore ave and rms values of freewheeling diode currents are zero.

(*d*) Rms value of output voltage $= \left[\dfrac{T_{on}}{T} \cdot V_s^2\right]^{1/2} = \sqrt{\alpha} \cdot V_s$

(*e*) Average thyristor current $= \dfrac{T_{on}}{T} \cdot \dfrac{V_s}{R} = \alpha \dfrac{V_s}{R}$

Rms thyristor current $= \left[\dfrac{T_{on}}{T} \cdot \left(\dfrac{V_s}{R}\right)^2\right]^{1/2} = \sqrt{\alpha} \cdot \dfrac{V_s}{R}$

(*f*) Average source current = average thyristor current = $\alpha \cdot \dfrac{V_s}{R}$

Effective input resistance of the chopper

Example 7.2. *For type-A chopper of Fig. 7.2 (a), dc source voltage = 230 V, load resistance = 10 Ω. Take a voltage drop of 2 V across chopper when it is on. For a duty cycle of 0.4, calculate*

(a) average and rms values of output voltage and

(b) chopper efficiency.

Solution. (*a*) When chopper is on, output voltage is $(V_s - 2)$ volts and during the time chopper is off, output voltage is zero.

$$\therefore \text{Average output voltage} = \frac{(V_s - 2)\, T_{on}}{T} = \alpha\,(V_s - 2)$$

$$= 0.4\,(230 - 2) = 91.2 \text{ V}$$

Rms value of output voltage,

$$V_{or} = \left[(V_s - 2)^2 \cdot \frac{T_{on}}{T}\right]^{1/2} = \sqrt{\alpha}\,(V_s - 2)$$

$$= \sqrt{0.4}\,(230 - 2) = 144.2 \text{ V}$$

(*b*) Power output or power delivered to load,

$$P_0 = \frac{V_{or}^2}{R} = \frac{(144.2)^2}{10} = 2079.364 \text{ W}$$

Power input to chopper, $P_i = V_s \cdot I_0 = 230 \times \frac{91.2}{10} = 2097.6$ W

Chopper efficiency $= \frac{P_0}{P_i} = \frac{2079.364}{2097.6} \times 100 = 99.13\%.$

Example 7.3. *A step-up chopper has input voltage of 220 V and output voltage of 660 V. If the non-conducting time of thyristor-chopper is 100 μs, compute the pulse width of output voltage.*

In case pulse width is halved for constant frequency operation, find the new output voltage.

Solution. From Eq. (7.5), $660 = 220 \frac{1}{1 - \alpha}$

or $\alpha = \frac{2}{3} = \frac{T_{on}}{T}$

$\therefore$ $T_{on} = \frac{2}{3} T$ and $T_{off} = T - T_{on} = \frac{1}{3} T = \frac{1}{3} T = 100$ μs (given)

$\therefore$ $T_{off} = 300$ μs and $T_{on} = \frac{2}{3} \times 300 = 200$ μs.

When pulse width is halved, $T_{on} = \frac{1}{2} \times 200 = 100$ μs

for constant frequency operation, $T = 300$ μs ; $T_{off} = T - T_{on} = 200$ μs

$$\alpha = \frac{T_{on}}{T} = \frac{100}{300} = \frac{1}{3}$$

$\therefore$ New output voltage, $V_0 = 220 \frac{1}{1 - \frac{1}{3}} = 330$ V.

7.4. TYPES OF CHOPPER CIRCUITS

Power semiconductor devices used in chopper circuits are unidirectional devices ; polarities of output voltage V_0 and the direction of output current I_0 are, therefore, restricted.

A chopper can, however, operate in any of the four quadrants by an appropriate arrangement of semiconductor devices. This characteristic of their operation in any of the four quadrants forms the basis of their classification as type-A chopper, type-B chopper etc. Some authors describe this chopper classification as class *A*, class *B*, ... in place of type-*A*, type-*B* .... respectively.

In the chopper-circuit configurations drawn henceforth, the current directions and voltage polarities marked in the power circuit would be treated as positive. In case current directions and voltage polarities turn out to be opposite to those shown in the circuit, these currents and voltages must be treated as negative.

In this section, the classification of various chopper configurations is discussed.

7.4.1. First-quadrant, or Type-A, Chopper

This type of chopper is shown in Fig. 7.6 (*a*). It is observed that chopper circuit of Fig. 7.2 (*a*) is also type-A chopper. In Fig. 7.6 (*a*), when chopper CH1 is on, $v_0 = V_s$ and current i_0 flows in the arrow direction shown. When CH1 is off , $v_0 = 0$ but i_0 in the load continues flowing in the same direction through freewheeling diode FD, Fig. 7.2 (*b*). It is thus seen that average values of both load voltage and current, *i.e.* V_0 and i_0 are always positive : this fact is shown by the hatched area in the first quadrant of $V_0 - I_0$ plane in Fig. 7.6 (*b*).

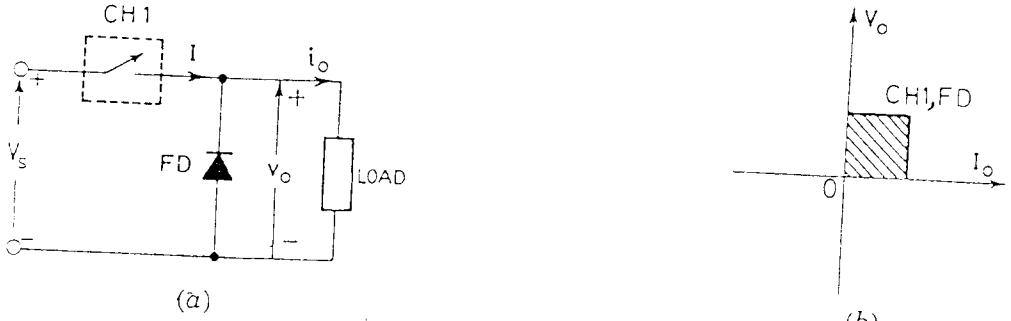


Fig. 7.6. First-quadrant, or type-A chopper.

The power flow in type-*A* chopper is always from source to load. This chopper is also called *step-down chopper* as average output voltage V_0 is always less than the input dc voltage V_s.

7.4.2. Second-quadrant, or Type-B, Chopper

Power circuit for this type of chopper is shown in Fig. 7.7 (*a*). Note that load must contain a dc source *E*, like a battery (or a dc motor) in this chopper.

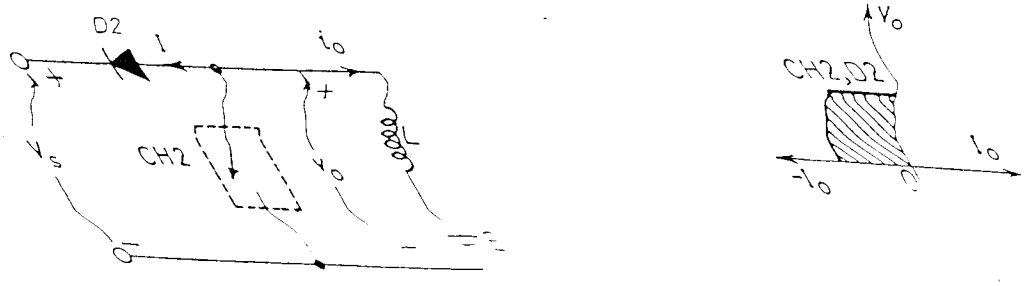


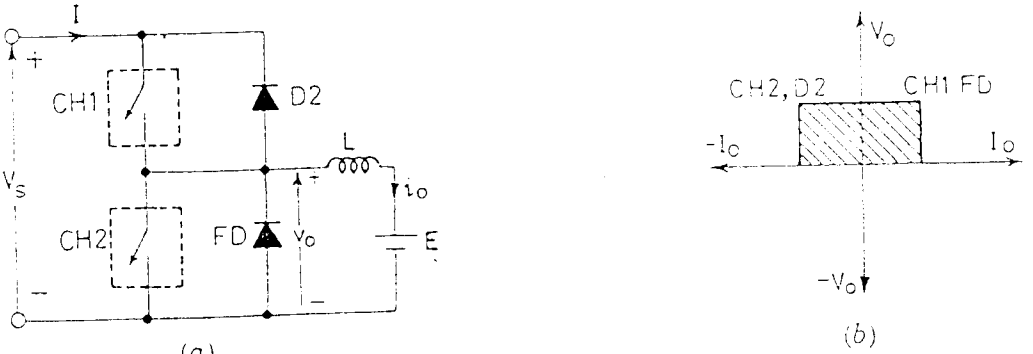
Fig. 7.7. Second-quadrant, or type-B chopper.

When CH2 is on, $v_0 = 0$ but load voltage E drives current through L and CH2. Inductance L stores energy during T_{on} (= on period) of CH2. When CH2 is off, $v_0 = \left(E + L\frac{di}{dt}\right)$ exceeds source voltage V_s. As a result, diode D2 is forward biased and begins conduction, thus allowing power to flow to the source. Chopper CH2 may be on or off, current I_0 flows out of the load, current i_0 is therefore treated as negative. Since V_0 is always positive and I_0 is negative, power flow is always from load to source. As load voltage $V_0 = \left(E + L\frac{di}{dt}\right)$ is more than source voltage V_s, type-B chopper is also called *step-up chopper*.

Both type-A and type-B chopper configurations have a common negative terminal between their input and output circuits.

7.4.3. Two-quadrant type-A chopper, or Type-C Chopper

This type of chopper is obtained by connecting type-A and type-B choppers in parallel as shown in Fig. 7.8 (a). The output voltage V_0 is always positive because of the presence of freewheeling diode FD across the load. When chopper CH2 is on, or freewheeling diode FD conducts, output voltage $v_0 = 0$ and in case chopper CH1 is on or diode D2 conducts, output voltage $v_0 = V_s$. The load current i_0 can, however, reverse its direction. Current i_0 flows in the arrow direction marked in Fig. 7.8 (a), *i.e.* load current is positive when CH1 is on or FD conducts. Load current is negative if CH2 is on or D2 conducts. In other words, CH1 and FD operate together as type-A chopper in first quadrant. Likewise, CH2 and D2 operate together as type-B chopper in second quadrant.



(a) (b)

Fig. 7.8. Two-quadrant type-A chopper, or type-C chopper.

Average load voltage is always positive but average load current may be positive or negative as explained above. Therefore, power flow may be from source to load (first-quadrant operation) or from load to source (second-quadrant operation). Choppers CH1 and CH2 should not be on simultaneously as this would lead to a direct short circuit on the supply lines. This type of chopper configuration is used for motoring and regenerative braking of dc motors. The operating region of this type of chopper is shown in Fig. 7.8 (b) by hatched area in first and second quadrants.

7.4.4. Two-quadrant Type-B Chopper, or Type-D Chopper

The power circuit diagram for two-quadrant type-B chopper, or type-D chopper, is shown in Fig. 7.9 (a). The output voltage $v_0 = V_s$ when both CH1 and CH2 are on and $v_0 = -V_s$ when both choppers are off but both diodes $D1$ and $D2$ conduct. Average output voltage V_0 is positive when choppers turn-on time T_{on} is more than their turn-off time T_{off} as shown in Fig. 7.9 (c). Average output voltage V_0 is negative when their $T_{on} < T_{off}$ Fig. 7.9 (d). The direction of load current is always positive because choppers and diodes can conduct current only in the

direction of arrows shown in Fig. 7.9 (*a*). As V_0 is reversible, power flow is reversible. The operation of this type of chopper is shown by the hatched area in first and fourth quadrants in Fig. 7.9 (*b*).

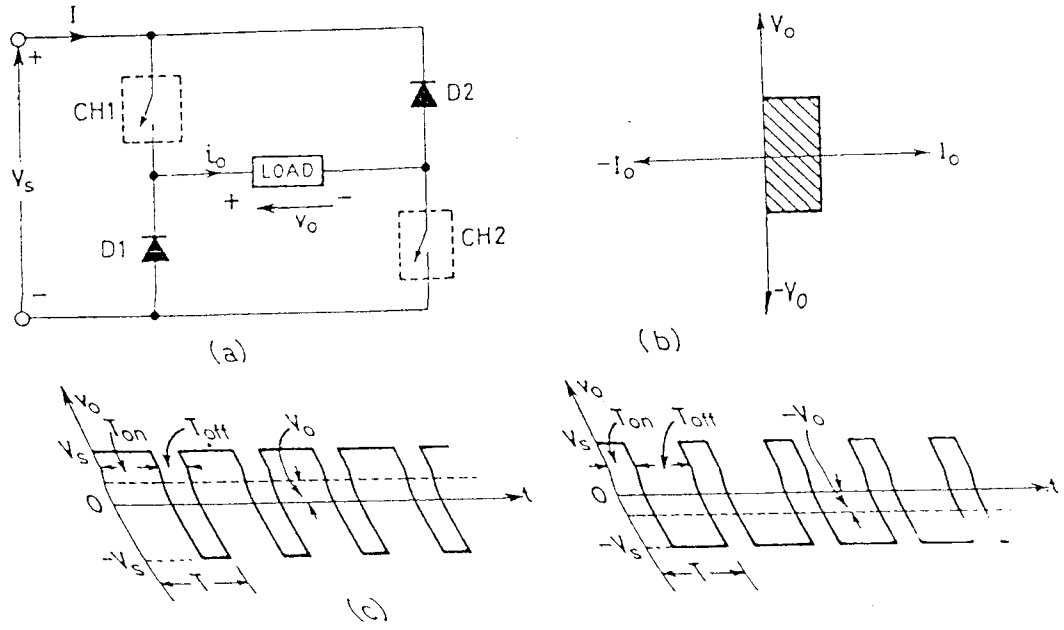


Fig. 7.9 (a) and (b) Two-quadrant type-B chopper. [illegible]
(c) V_0 is positive, $T_{on} > T_{off}$ and (d) V_0 is negative [illegible]

7.4.5. Four-quadrant Chopper, or Type-E Chopper

The power circuit diagram for a four-quadrant chopper is shown in Fig. [illegible] of four semiconductor switches CH1 to CH4 and four diodes D1 to D4 in anti-parallel. The operation of this chopper in the four quadrants is explained as under :

First quadrant : *For first-quadrant operation of Fig. 7.10 (a), CH4 is kept on, CH3 is kept off and CH1 is operated. With CH1, CH4 on, load voltage $v_0 = V_s$ is applied to the load current i_0 begins to flow. Here both v_0 and i_0 are positive giving first quadrant operation. When CH1 is turned off, positive current freewheels through CH4, D2. In this manner both* V_0, I_0 can be controlled in the first quadrant.

Second quadrant : *Here CH2 is operated* and CH1, CH3 and CH4 are kept off. With CH2 on, reverse (or negative) current flows through L, CH2, D4 and E. Inductance L stores energy during the time CH2 is on. When CH2 is turned off, current is fed back to source through diodes D1, D4. Note that here $\left(E + L\frac{di}{dt}\right)$ is more than the source voltage V_s. As load voltage V_0 is positive and I_0 is negative, it is second quadrant operation of chopper. Also power is fed back from load to source.

Third quadrant : For third-quadrant operation of Fig. 7.10 (*a*), CH1 is kept off, CH2 is kept on and *CH3 is operated.* Polarity of load emf E must be reversed for this quadrant working. With CH3 on, load gets connected to source V_s so that both v_0, i_0 are negative leading to third quadrant operation. When CH3 is turned off, negative current freewheels through CH2, D4. In this manner, v_0 and i_0 can be controlled in the third quadrant.

Fourth quadrant : *Here CH4 is operated* and other devices are kept off. Load emf E [illegible]

direction of arrows shown in Fig. 7.9 (*a*). As V_0 is reversible, power flow is reversible. The operation of this type of chopper is shown by the hatched area in first and fourth quadrants in Fig. 7.9 (*b*).

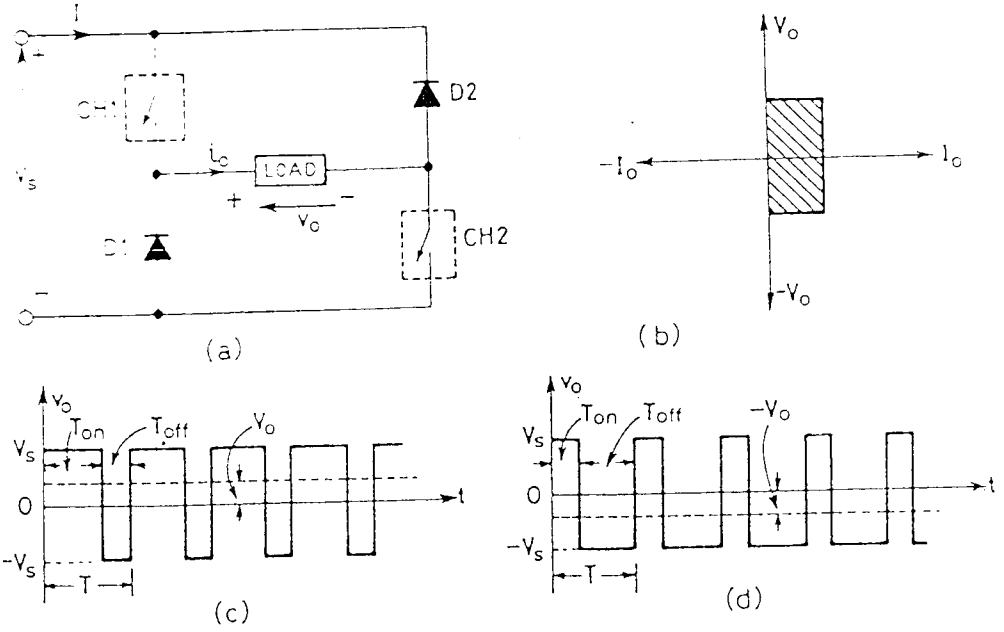


Fig. 7.9 (*a*) and (*b*) Two-quadrant type-B chopper, or type-D chopper
(*c*) V_0 is positive, $T_{on} > T_{off}$ and (*d*) V_0 is negative, $T_{on} < T_{off}$.

7.4.5. Four-quadrant Chopper, or Type-E Chopper

The power circuit diagram for a four-quadrant chopper is shown in Fig. 7.10 (*a*). It consists of four semiconductor switches CH1 to CH4 and four diodes D1 to D4 in antiparallel. Working of this chopper in the four quadrants is explained as under :

First quadrant : For first-quadrant operation of Fig. 7.10 (*a*), CH4 is kept on, CH3 is kept off and *CH1 is operated.* With CH1, CH4 on, load voltage $v_0 = V_s$ (source voltage) and load current i_0 begins to flow. Here both v_0 and i_0 are positive giving first quadrant operation. When CH1 is turned off, positive current freewheels through CH4, D2. In this manner, both V_0, I_0 can be controlled in the first quadrant.

Second quadrant : *Here CH2 is operated* and CH1, CH3 and CH4 are kept off. With CH2 on, reverse (or negative) current flows through L, CH2, D4 and E. Inductance L stores energy during the time CH2 is on. When CH2 is turned off, current is fed back to source through diodes D1, D4. Note that here $\left(E + L\frac{di}{dt}\right)$ is more than the source voltage V_s. As load voltage V_0 is positive and I_0 is negative, it is second quadrant operation of chopper. Also power is fed back from load to source.

Third quadrant : For third-quadrant operation of Fig. 7.10 (*a*), CH1 is kept off, CH2 is kept on and *CH3 is operated.* Polarity of load emf E must be reversed for this quadrant working. With CH3 on, load gets connected to source V_s so that both v_0, i_0 are negative leading to third quadrant operation. When CH3 is turned off, negative current freewheels through CH2, D4. In this manner, v_0 and i_0 can be controlled in the third quadrant.

Fourth quadrant : *Here CH4 is operated* and other devices are kept off. Load emf E

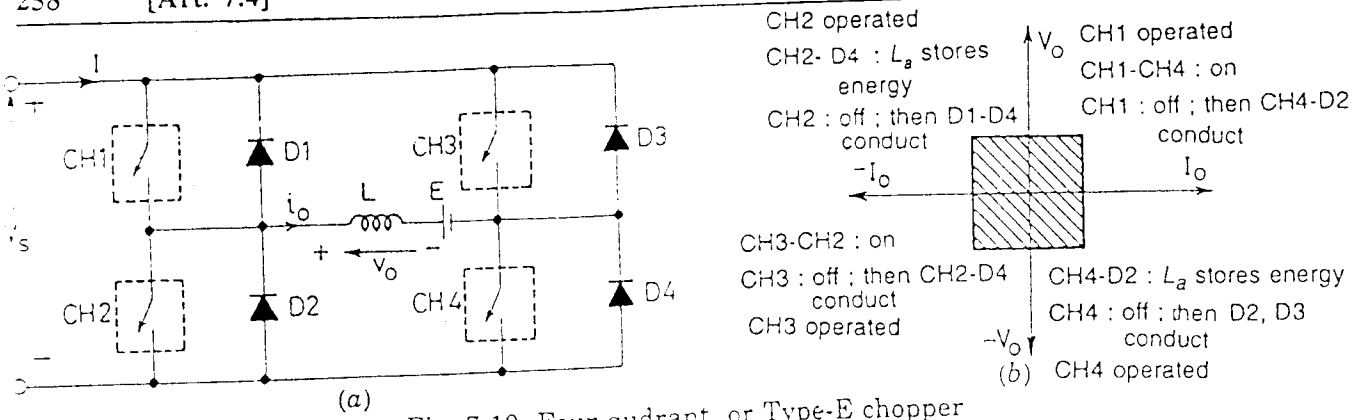


Fig. 7.10. Four-qudrant, or Type-E chopper
(a) circuit diagram and (b) operation of conducting devices.

quadrant. With CH4 on, positive current flows through CH4, D2, L and E. Inductance L stores energy during the time CH4 is on. When CH4 is turned off, current is fed back to source through diodes D2, D3. Here load voltage is negative, but load current is positive leading to the chopper operation in the fourth quadrant. Also power is fed back from load to source.

The devices conducting in the four quadrants are indicated in Fig. 7.10 (b).

Example 7.4. *Show that for a basic dc to dc converter, the critical inductance of the filter circuit is given by*

$$L = \frac{V_0^2 (V_s - V_0)}{2f V_s P_0}$$

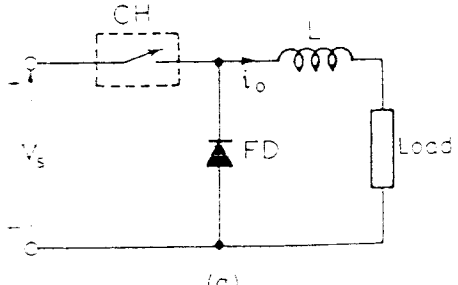
where V_0, V_s, P_0 and f are load voltage, source voltage, load power and chopping frequency respectively.

Solution. The critical inductance L is that value of inductance for which the output current falls to zero at $t = T$ during the turn-off period of the chopper. A typical waveform of output current, with critical inductance in the load circuit, is shown in Fig. 7.11 (b). If current variation, from zero to I_{mx} during T_{on} and from I_{mx} to zero during T_{off}, is assumed linear, then average value of output current I_0 is given by

$$I_0 \cdot T = \frac{1}{2} I_{mx} T_{on} + \frac{1}{2} I_{mx} T_{off}$$

$$= \frac{1}{2} I_{mx} \left(T_{on} + T_{off} \right) = \frac{1}{2} I_{mx} T$$

or $I_{mx} = 2 I_0$ = maximum value of chopper current at $t = T_{on}$. It is seen from Fig. 7.11 (a) that when chopper CH is on,



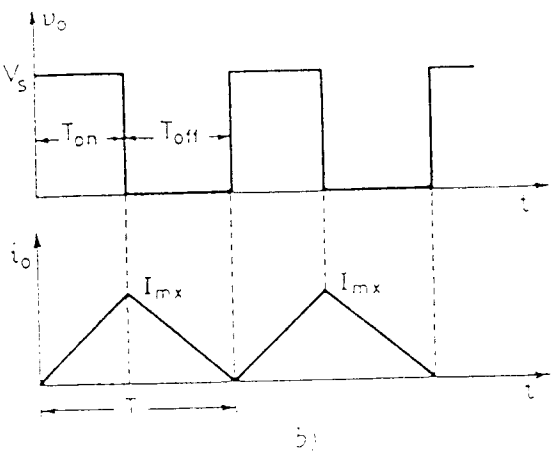


Fig. 7.11. Pertaining to Example 7.4

$$V_0 + L\frac{di}{dt} = V_s \quad \text{or} \quad V_0 + L\frac{I_{mx}}{T_{on}} = V_s$$

or
$$L\frac{2I_0}{T_{on}} = V_s - V_0$$

$\therefore$
$$L = \frac{(V_s - V_0)\,T_{on}}{2I_0}$$

But average value of output voltage $V_0 = f\,T_{on}\,V_s$ and output, or load, power $P_0 = V_0$ This gives

$$T_{on} = \frac{V_0}{f \cdot V_s} \text{ and } I_0 = \frac{P_0}{V_0}$$

Substituting these values of T_{on} and I_0 in Eq (*i*), we get

$$L = \frac{(V_s - V_0)\,V_0^2}{2f\,V_s\,P_0}$$

7.5. STEADY STATE TIME-DOMAIN ANALYSIS OF TYPE-A CHOPPER

For the type-*A* chopper of Fig. 7.6 (*a*) with *RLE* load, the waveforms for gate signal load current i_0 and load voltage v_0 are as shown in Fig. 7.12 (*a*) for continuous conduction and, in Fig. 7.12 (*b*) for discontinuous conduction. In Fig. 7.12 (*b*), periodic time T is than that in Fig. 7.12 (*a*). The determination of load current expression is useful for kn (*i*) the current profile over periodic time T, (*ii*) the current ripple and (*iii*) whether the is continuous or discontinuous. The object of this article is to study the type-A chopper *RLE* load for current variation over T, current ripple and also for the Fourier analysis output voltage.

For *RLE* type load, E is the load voltage which may be a dc motor or a battery. CH1 is on in Fig. 7.6 (*a*), the equivalent circuit is as shown in Fig. 7.12 (*c*). For this mode operation, the differential equation governing its performance is

$$V_s = R\,i + L\frac{di}{dt} + E$$

for
$$0 \le t \le T_{on}.$$

When CH1 is off, the load current continues flowing through the freewheeling diode the equivalent circuit is as shown in Fig. 7.12 (*d*). For this circuit, the differential equation is

$$0 = R\,i + L\frac{di}{dt} + E$$

for
$$T_{on} < t \le T.$$

Solution of Eqs. (7.6) and (7.7) may be obtained by the use of Laplace transform. It is seen from Fig. 7.12 (*a*) that initial value of current is I_{mn} for Eq. (7.6) and I_{mx} for Eq. Therefore, Laplace transform of Eqs. (7.6) and (7.7) is

$$RI(s) + L[sI(s) - I_{mn}] = \frac{V_s - E}{s}$$

and
$$RI(s) + L[sI(s) - I_{mx}] - \frac{E}{s}$$

From Eq. (7.8),
$$I(s) = \frac{V_s - E}{s(R + L_s)} + \frac{L \cdot I_{mn}}{R + L_s} = \frac{V_s - E}{\left(\quad R\right)} + \frac{I_{mn}}{R}$$

EIGHT

Inverters

A device that converts dc power into ac power at desired output voltage and frequency is called an inverter. Some industrial applications of inverters are for adjustable-speed ac drives, induction heating, stand by air-craft power supplies, UPS (uninterruptible power supplies) for computers, hvdc transmission lines etc. Phase-controlled converters, when operated in the inverter mode, are called line-commutated inverters, Chapter 6. But line-commutated inverters require at the output terminals an existing ac supply which is used for their commutation. This means that line-commutated inverters can't function as isolated ac voltage sources or as variable frequency generators with dc power at the input. Therefore, voltage level, frequency and waveform on the ac side of line-commutated inverters cannot be changed. On the other hand, force commutated inverters provide an independent ac output voltage of adjustable voltage and adjustable frequency and have therefore much wider applications. In this chapter, force-commutated and load commutated inverters are described.

The dc power input to the inverter is obtained from an existing power supply network or from a rotating alternator through a rectifier or a battery, fuel cell, photovoltaic array or magneto hydrodynamic (MHD) generator. The configuration of ac to dc converter and dc to ac inverter is called a dc-link converter. The rectification is carried out by standard diodes or thyristor converter circuits discussed in Chapter 6. The inversion is performed by the methods discussed in this chapter.

Inverters can be broadly classified into two types ; voltage source inverters and current source inverters. A voltage-fed inverter (VFI), or voltage-source inverter (VSI), is one in which the dc source has small or negligible impedance. In other words, a voltage source inverter has stiff dc voltage source at its input terminals. A current-fed inverter (CFI) or current-source inverter (CSI) is fed with adjustable current from a dc source of high impedance, *i.e.* from a stiff dc current source. In a CSI fed with stiff current source, output current waves are not affected by the load.

In VSIs using thyristors, some type of forced commutation is usually required. In case VSIs are made up of using GTOs, power transistors, power MOSFETS or IGBTs *self-commutation* with base or gate drive signals is employed for their controlled turn-on and turn-off.

The object of this chapter is to describe the operating principles of both single-phase and three-phase inverters and to present their elementary analysis. As before, switching devices are assumed to possess ideal characteristics.

8.1. SINGLE-PHASE VOLTAGE SOURCE INVERTERS : OPERATING PRINCIPLE

In this section, operating principle of single-phase voltage source inverters is discussed.

8.1.1. Single-phase Bridge Inverters

Single-phase bridge inverters are of two types, namely (*i*) single-phase half-bridge inverters and (*ii*) single-phase full-bridge inverters. Basic principles of operation of these two types are presented here.

Power circuit diagrams of the two configurations of single-phase bridge inverter, as stated above, are shown in Fig. 8.1 (*a*) for half-bridge inverter and in Fig. 8.2 (*a*) for full-bridge inverter. In these diagrams, the circuitry for turning-on or turning-off of the thyristors is not shown for simplicity. The gating signals for the thyristors and the resulting output voltage waveforms are shown in Figs. 8.1 (*b*) and 8.2 (*b*) for half-bridge and full-bridge inverters respectively. These voltage waveforms are drawn on the assumption that each thyristor conducts for the duration its gate pulse is present and is commutated as soon as this pulse is removed. In Figs. 8.1 (*b*) and 8.2 (*b*), $i_{g1} - i_{g4}$ are gate signals applied respectively to thyristors T1-T4.

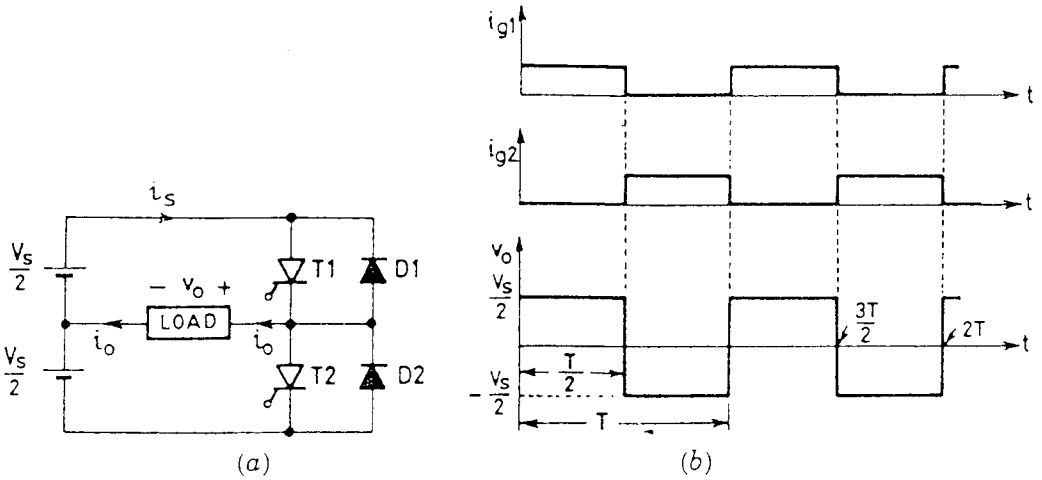


Fig. 8.1. Single-phase half-bridge inverter.

Single-phase half bridge inverter, as shown in Fig. 8.1 (*a*), consists of two SCRs, two diodes and three-wire supply. It is seen from Fig. 8.1 (*b*) that for $0 < t \leq T/2$, thyristor T1

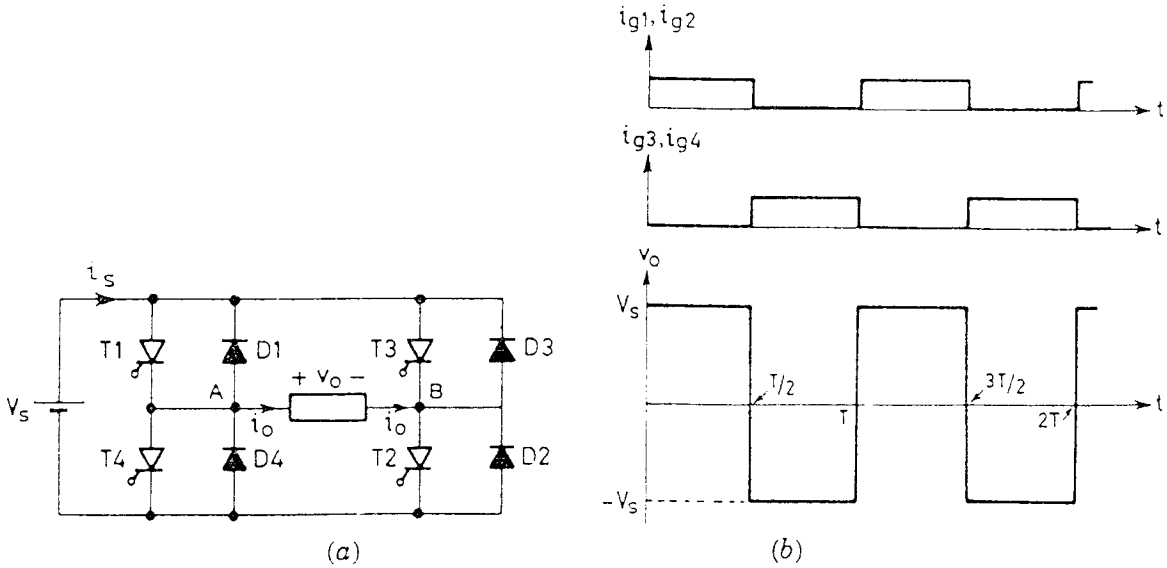


Fig. 8.2. Single-phase full-bridge inverter.

conducts and the load is subjected to a voltage $V_s/2$ due to the upper voltage source $V_s/2$. At $t = T/2$, thyristor T1 is commutated and T2 is gated on. During the period $T/2 < t \leq T$, thyristor T2 conducts and the load is subjected to a voltage $(-V_s/2)$ due to the lower voltage source $V_s/2$. It is seen from Fig. 8.1 (*b*) that load voltage is an alternating voltage waveform of amplitude $V_s/2$ and of frequency $1/T$ Hz. Frequency of the inverter output voltage can be changed by controlling T.

The main drawback of half-bridge inverter is that it requires 3-wire dc supply. This difficulty can, however, be overcome by the use of a full-bridge inverter shown in Fig. 8.2 (*a*). It consists of four SCRs and four diodes. In this inverter, number of thyristors and diodes is twice of that in a half bridge inverter. This, however, does not go against full inverter because the amplitude of output voltage as well as its output power is doubled in this inverter as compared to their values in the half-bridge inverter. This is evident from Figs. 8.1 (*b*) and 8.2 (*b*).

For full-bridge inverter, when T1, T2 conduct, load voltage is V_s and when T3, T4 conduct load voltage is $-V_s$ as shown in Fig. 8.2 (*b*). Frequency of output voltage can be controlled by varying the periodic time T.

In Fig. 8.1 (*a*), thyristors T1, T2 are in series across the source ; in Fig. 8.2 (*a*) thyristors T1, T4 or T3, T2 are also in series across the source. During inverter operation, it should be ensured that two SCRs in the same branch, such as T1, T2 in Fig. 8.1 (*a*), do not conduct simultaneously as this would lead to a direct short circuit of the source.

For a resistive load, two SCRs in Fig. 8.1 (*a*) and four SCRs in Fig. 8.2 (*a*) would suffice, because load current i_0 and load voltage v_0 would always be in phase with each other. This, however, is not the case when the load is other than resistive. For such types of loads, current i_0 will not be in phase with voltage v_0 and diodes connected in antiparallel with thyristors will allow the current to flow when the main thyristors are turned off. These diodes are called *feedback diodes*.

8.1.2. Steady-state Analysis of Single-phase Inverter

Figs. 8.1 (*b*) and 8.2 (*b*) reveal that load voltage waveform does not depend on the nature of load. The load voltage is given by

for half-bridge inverter, $$v_0 = \frac{V_s}{2} \quad \ldots\ldots 0 < t << T/2$$

$$= -\frac{V_s}{2} \quad \ldots\ldots T/2 < t < T$$

and for full-bridge inverter, $$v_0 = V_s \quad \ldots\ldots 0 < t < T/2$$

$$= -V_s \quad \ldots\ldots T/2 < t < T$$

The load current is, however, dependent upon the nature of load. Let the load, in general, consist of RLC in series. The circuit model of single-phase half-bridge or full-bridge inverter is as shown in Fig. 8.3 (*a*). In this circuit, load current would finally settle down to steady state conditions and would vary periodically as shown in Figs. 8.3 (*c*) to (*f*). It is seen from these waveforms that

$$i_0 = -I_0 \quad \ldots\ldots \text{at } t = 0, T, 2T, 3T, \ldots\ldots$$

and $$i_0 = I_0 \quad \ldots\ldots \text{at } t = T/2, 3T/2, 5T/2, \ldots\ldots$$

Now, the circuit model of Fig. 8.3 (*a*) for half-bridge inverter and for

8.1. SINGLE-PHASE VOLTAGE SOURCE INVERTERS : OPERATING PRINCIPLE

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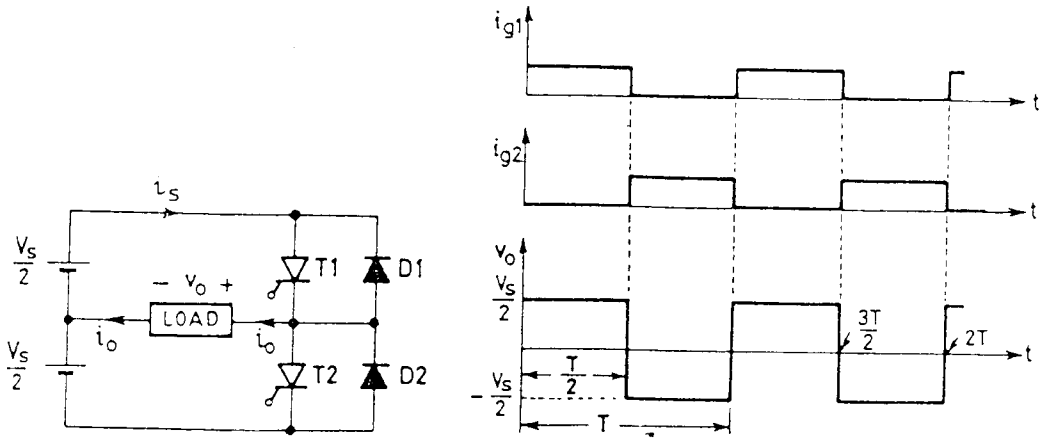
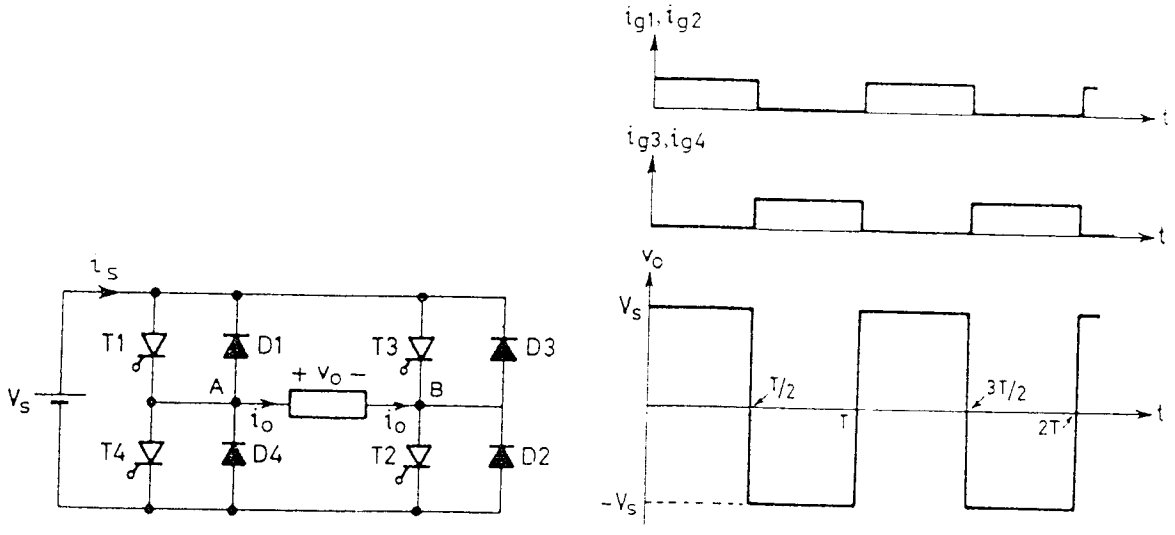


(*a*) (*b*)

Fig. 8.1. Single-phase half-bridge inverter.

Single-phase half bridge inverter, as shown in Fig. 8.1 (*a*), consists of two SCRs, two diodes and three-wire supply. It is seen from Fig. 8.1 (*b*) that for $0 < t \leq T/2$, thyristor T1



(*a*) (*b*)

Fig. 8.2. Single-phase full-bridge inverter.

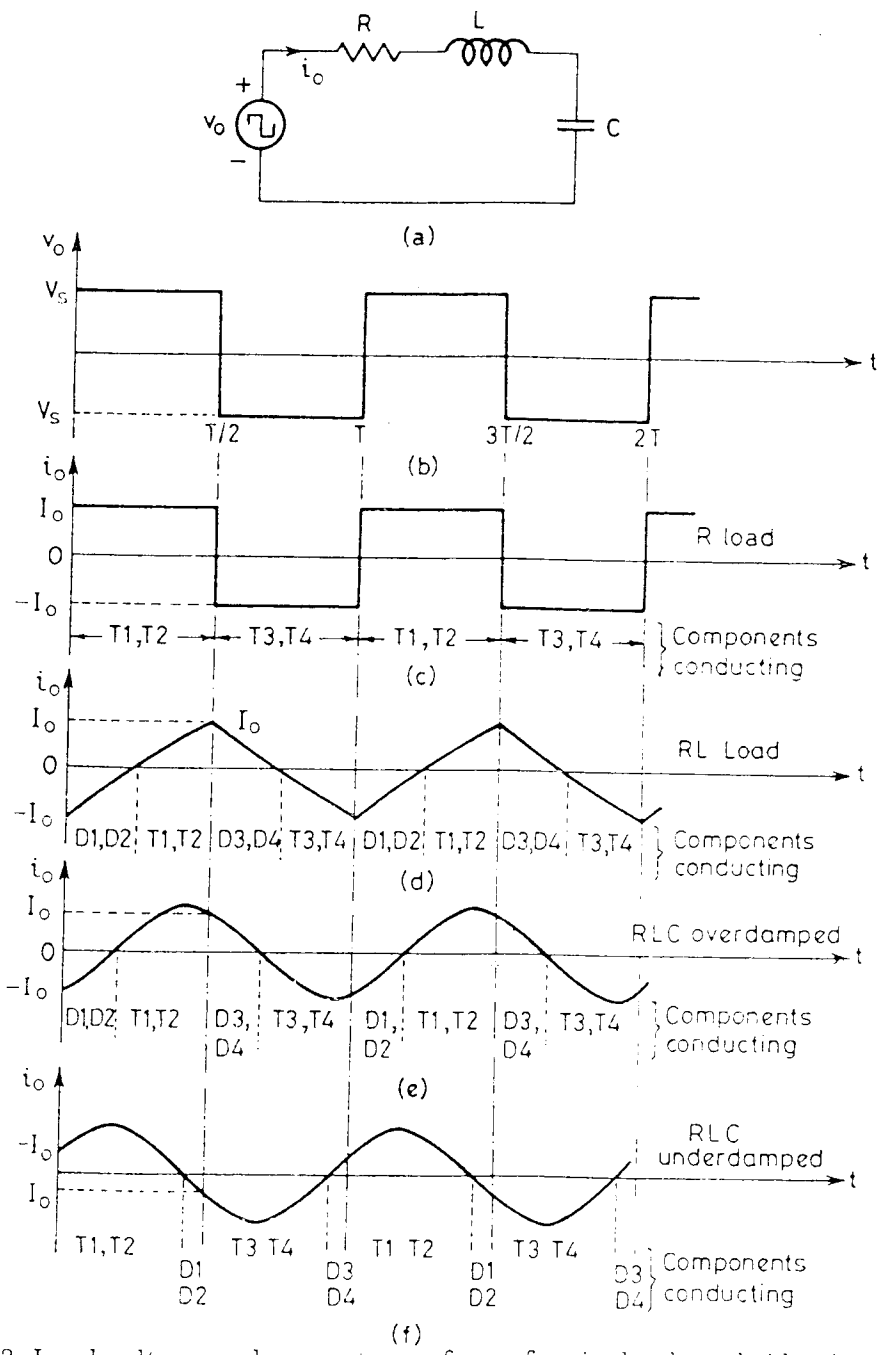


Fig. 8.3. Load voltage and current waveforms for single-phase bridge inverter.

$$\frac{V_s}{2} = R\, i_0 + L\, \frac{d\, i_0}{dt} + \frac{1}{C} \int i_0 dt + V_{c1} \qquad \ldots(8.1)$$

For full-bridge inverter, replace $V_s/2$ by V_s in Eq. (8.1). In this equation, V_{c1} is the initial voltage across capacitor at $t = 0$.

For $T/2 < t < T$, or $0 < t' < T/2$, the voltage equation for half-bridge inverter is

$$-\frac{V_s}{2} = R\, i_0 + L\, \frac{di}{dt'} + \frac{1}{C} \int i dt' + V_{c2} \qquad \ldots(8.2)$$

and for a full-bridge inverter, replace $(-V_s/2)$ by $(-V_s)$ in Eq. (8.2). In this equation, V_{c2} is the initial voltage across capacitor at $t = 0$

Differentiation of Eqs. (8.1) and (8.2) gives

$$\frac{d^2 i_0}{dt^2} + \frac{R}{L}\frac{d i_0}{dt} + \frac{1}{LC} i_0 = 0$$

and

$$\frac{d^2 i_0}{dt'^2} + \frac{R}{L}\frac{d i_0}{dt'} + \frac{1}{LC} i_0 = 0$$

The solution of these second order differential equations can be obtained by using initial conditions as specified above. Components constituting the load decide the nature of load current waveforms.

For a full inverter, the rectangular output voltage waveform is shown in Fig. 8.3 (*b*). For this inverter, various current waveforms for different load characteristics are drawn in Fig. 8.3 (*c*) to (*f*). The nature of these current waveforms is briefly discussed in what follows :

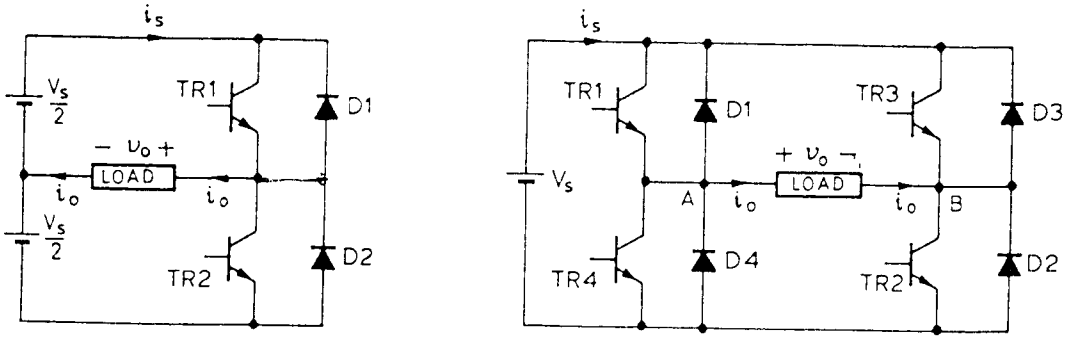
R load. For a resistive load R, load current waveform i_0 is identical with load voltage waveform v_0 and diodes D1-D4 do not come into conduction, Fig. 8.3 (*c*).

RL and RLC overdamped loads. The load current waveforms for RL and RLC overdamped loads are shown in Figs. 8.3 (*d*) and (*e*) respectively. Before $t = 0$, thyristors T3, T4 are conducting and load current i_0 is flowing from B to A, *i.e.* in the reversed direction, Fig. 8.2 (*a*). This current is shown as $-I_0$ at $t = 0$ in Figs. 8.3 (*d*) and (*e*). After T3, T4 are turned off at $t = 0$, current i_0 cannot change its direction immediately because of the nature of load. As a result, diodes D1, D2 start conducting after $t = 0$ and allow i_0 to flow against the supply voltage V_s. As soon as D1, D2 begin to conduct, load is subjected to V_s as shown. Though T1, T2 are gated at $t = 0$, these SCRs will not turn on as these are reverse biased by voltage drops across diodes D1 and D2. When load current through $D1$, $D2$ falls to zero, T1 and T2 become forward biased by source voltage V_s, T1 and T2 therefore get turned on as these are gated for a period $T/2$ sec. Now load current i_0 flows in the positive direction from A to B. At $t = T/2$; T1, T2 are turned off by forced commutation and as load current cannot reverse immediately, diodes D3, D4 come into conduction to allow the flow of current i_0 after $T/2$.

Thyristors T3, T4, though gated, will not turn on as these are reverse biased by the voltage drop in diodes D3, D4. When current in diodes D3, D4 drops to zero ; T3, T4 are turned on as these are already gated. The conduction of various components of the full-bridge inverter is shown in Figs. 8.3 (*d*) and (*e*).

RLC underdamped load. The load current i_0 for RLC underdamped load is shown in Fig. 8.3 (*f*). After $t = 0$; T1, T2 are conducting the load current. As i_0 through T1, T2 reduces to zero at t_1, these SCRs are turned off before T3, T4 are gated. As T1, T2 stop conducting, current through the load reverses and is now carried by diodes D1, D2 as T3, T4 are not yet gated. The diodes D1, D2 are connected in antiparallel to T1, T2 ; the voltage drop in these diodes appears as a reverse bias across T1, T2. If duration of this reverse bias is more than the SCR turn-off time t_q, *i.e.* If $(T/2 - t_1) > t_q$; T1, T2 will get commutated naturally and therefore no commutation circuitry will be needed. This method of commutation, knows as *load commutation*, is in fact used in high frequency inverters used for induction heating.

In single-phase bridge inverters shown in Figs. 8.1 (*a*) and 8.2 (*a*), thyristors are shown as switching devices. Note that basic inverter operation is not dependent on the particular semiconductor device used. It means that if *npn* transistors (or GTOs, IGBTs etc.) are used



(*a*) (*b*)

Fig. 8.4. Single-phase (*a*) half-bridge and (*b*) full-bridge inverters using transistors.

obtained. The operating principle of an inverter using transistors, Fig. 8.4, can be described merely replacing T (for thyristor) by TR (for transistor) in Figs. 8.1 (*b*), 8.2 (*b*) and 8.3 (*c* to *f*).

Example. 8.1. *(a) A single-phase full bridge inverter is connected to an RL load. For a dc source voltage of V_s and output frequency $f = 1/T$, obtain expressions for load current as a function of time for the first two half cycles of the output voltage.*

(b) Derive also the expressions for steady-state current for the first two half cycles.

(c) For $R = 20\ \Omega$ and $L = 0.1\ H$, obtain current expressions for parts (a) and (b) in case source voltage is 240 V dc and frequency of output voltage is 50 Hz.

Solution. (*a*) For the first half cycle, Fig. 8.3 (*b*), *i.e.* for $0 < t < T/2$, the voltage equation for *RL* load is

$$V_s = Ri_0 + L\frac{di_0}{dt} \qquad ...(8.3)$$

Its Laplace transform, with zero initial conditions, is

$$\frac{V_s}{s} = R\,I(s) + Ls \cdot I(s) = I(s)\,[R + Ls]$$

Its time solution is,

$$i_0(t) = \frac{V_s}{R}\left(1 - e^{-\frac{R}{L}t}\right) \qquad ...(8.4)$$

for $0 < t < T/2.$

This is the expression of current as a function of time for the first half cycle from the instant of switching in with $i_0(t) = 0$ at $t = 0$.

At $t = T/2$, current $i_0(t)$ of Eq. (8.4) becomes the initial value for second half cycle.

$$\therefore \qquad i_0(T/2) = \frac{V_s}{R}\left(1 - e^{-\frac{RT}{2L}}\right) \qquad ...(8.5)$$

For second half cycle, time limit is from $T/2$ to T or $0 < t' < T/2$ where $t' = t - T/2$. The voltage equation for *RL* load during second half cycle is

$$-V_s = R\,i_0 + L\frac{di_0}{dt'} \qquad ...(8.6)$$

Its Laplace transform, with initial current $i_0\,(T/2)$ given by Eq. (8.5), is

$$-\frac{V_s}{s} = I(s)\,[R + Ls] - i_0(T/2) \cdot L$$

or $$I(s) = -\frac{V_s}{s(R+Ls)} + \frac{L \cdot i_0(T/2)}{R+Ls}$$

Its time solution is $$i_0(t') = -\frac{V_s}{R}\left(1 - e^{-\frac{R}{L}t'}\right) + i_0(T/2)e^{-\frac{R}{L}t'}$$

$$= -\frac{V_s}{R}\left(1 - e^{-\frac{R}{L}t'}\right) + \frac{V_s}{R}\left(1 - e^{-\frac{RT}{2L}}\right)e^{-\frac{R}{L}t'}$$

or $$i_0(t') = -\frac{V_s}{R} + \frac{V_s}{R}\left(2 - e^{-\frac{RT}{2L}}\right)e^{-\frac{R}{L}t'} \quad ...(8.7)$$

for $$0 < t' < T/2.$$

Eqs. (8.4) and (8.7) give the transient solution for load current for first and second half cycles respectively.

(*b*) Under steady-state conditions, at $t = 0$, $i_0(0) = -I_0$, Fig. 8.3 (*d*). Under this condition, Laplace transform of Eq. (8.3), is

$$\frac{V_s}{s} = I(s)\,[R + Ls] + L\,I_0$$

Its time solution is $$i_0(t) = \frac{V_s}{R}\left(1 - e^{-\frac{R}{L}t}\right) - I_0\,e^{-\frac{R}{L}t} \quad ...(8.8)$$

At $t = T/2$, $i_0(t) = I_0$ Fig. 8.3 (*d*), therefore from Eq. (8.8)

$$i_0(T/2) = I_0 = \frac{V_s}{R}\left(1 - e^{-\frac{RT}{2L}}\right) - I_0 \cdot e^{-\frac{RT}{2L}}$$

or $$I_0 = \frac{V_s}{R} \cdot \frac{1 - e^{-\frac{RT}{2L}}}{1 + e^{-\frac{RT}{2L}}} \quad ...(8.9)$$

Substituting this value of I_0 in Eq. (8.8), gives

$$i_0(t) = \frac{V_s}{R}\left(1 - e^{-\frac{R}{L}t}\right) - \frac{V_s}{R}\,\frac{1 - e^{-\frac{RT}{2L}}}{1 + e^{-\frac{RT}{2L}}}\,e^{-\frac{R}{L}t} \quad ...(8.10)$$

Eq. (8.10), gives the steady-state solution during the first half cycle, *i.e.* for $0 < t < T/2$.

For second half cycle, at $t = T/2$, $i_0(T/2) = I_0$, Fig. 8.3 (*d*). Under this initial condition, Laplace transform of Eq. (8.6), is

$$-\frac{V_s}{R} = I(s)\,[R + Ls] - L\,I_0$$

Its time solution is $$i_0(t) = -\frac{V_s}{R}\left(1 - e^{-\frac{R}{L}t'}\right) + I_0\,e^{-\frac{R}{L}t'}$$

$$= -\frac{V_s}{R}\left(1 - e^{-\frac{R}{L}t'}\right) + \frac{V_s}{R} \cdot \frac{1 - e^{-\frac{RT}{2L}}}{1 + e^{-\frac{RT}{2L}}} \cdot e^{-\frac{R}{L}t'} \quad ...(8.11)$$

Eq. (8.11) gives the steady-state solution during the second half cycle, *i.e.* for $0 < t' < T/2$ where $t' = t - T/2$.

(*c*) Here $\frac{R}{L} = \frac{200}{0.1} = 2000$, $\frac{1}{L} = \frac{1}{0.1} = 10$, $\frac{RT}{2L} = \frac{2000}{100}$

are double of those in the half-bridge inverter of Fig. 8.15. The working of this inverter is similar to that described for half-bridge inverter in the previous section. For example, for mode I, thyristors T1, T2 are conducting and load current flows through V_s, T1, L1, load, L2, T2. Voltage across C1, C2 is zero but C3, C4 are charged to voltage V_s. For initiating commutation of T1, T2 ; thyristors T3, T4 are triggered. This reverse biases T1, T2 by voltage $-V_s$, these thyristors are therefore turned off and so on.

8.4. THREE PHASE BRIDGE INVERTERS

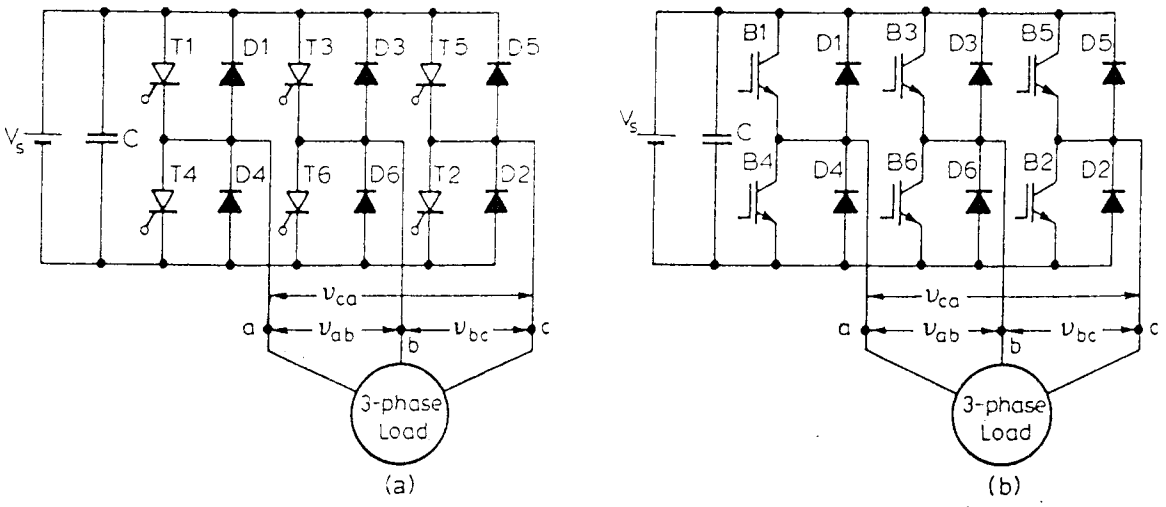
For providing adjustable-frequency power to industrial applications, three-phase inverters are more common than single-phase inverters. Three-phase inverters, like single-phase inverters, take their dc supply from a battery or more usually from a rectifier.

A basic three-phase inverter is a six-step bridge inverter. It uses a minimum of six thyristors. In inverter terminology, a step is defined as a change in the firing from one thyristor to the next thyristor in proper sequence. For one cycle of 360°, each step would be of 60° interval for a six-step inverter. This means that thyristors would be gated at regular intervals of 60° in proper sequence so that a 3-phase ac voltage is synthesized at the output terminals of a six-step inverter.

Fig. 8.19 (*a*) shows the power circuit of a three-phase bridge inverter using six thyristors and six diodes. As stated earlier, the transistor family of devices is now very widely used in inverter circuits. Presently, the use of IGBTs in single-phase and three-phase inverters is on the rise. The basic circuit configuration of inverter, however, remains unaltered as shown in Fig. 8.19 (*b*) for a three-phase bridge inverter using IGBTs in place of thyristors. A large capacitor connected at the input terminals tends to make the input dc voltage constant. This capacitor also suppresses the harmonics fed back to the source.

In Fig. 8.19 (*a*) inverter using six thyristors, commutation and snubber circuits are omitted for simplicity. It may be seen from Figs. 8.1 and 8.19 that a three-phase bridge inverter consists of three half-bridge inverters arranged side by side. The three-phase load is assumed to be star connected. In Fig. 8.19 (*a*), the thyristors are numbered in the sequence in which they are triggered to obtain voltages v_{ab}, v_{bc}, v_{ca} at the output terminals *a*, *b*, *c* of the inverter.

There are two possible patterns of gating the thyristors. In one pattern, each thyristor conducts for 180° and in the other, each thyristor conducts for 120°. But in both these patterns,



gating signals are applied and removed at 60° intervals of the output voltage waveform. Therefore, both these modes require a six step bridge inverter. These modes of thyristor conduction are described in what follows :

8.4.1. Three-phase 180 Degree Mode VSI

In the three-phase inverter of Fig. 8.19, each SCR conducts for 180° of a cycle. Thyristor pair in each arm, *i.e.* T1, T4 ; T3, T6 and T5, T2 are turned on with a time interval of 180°.

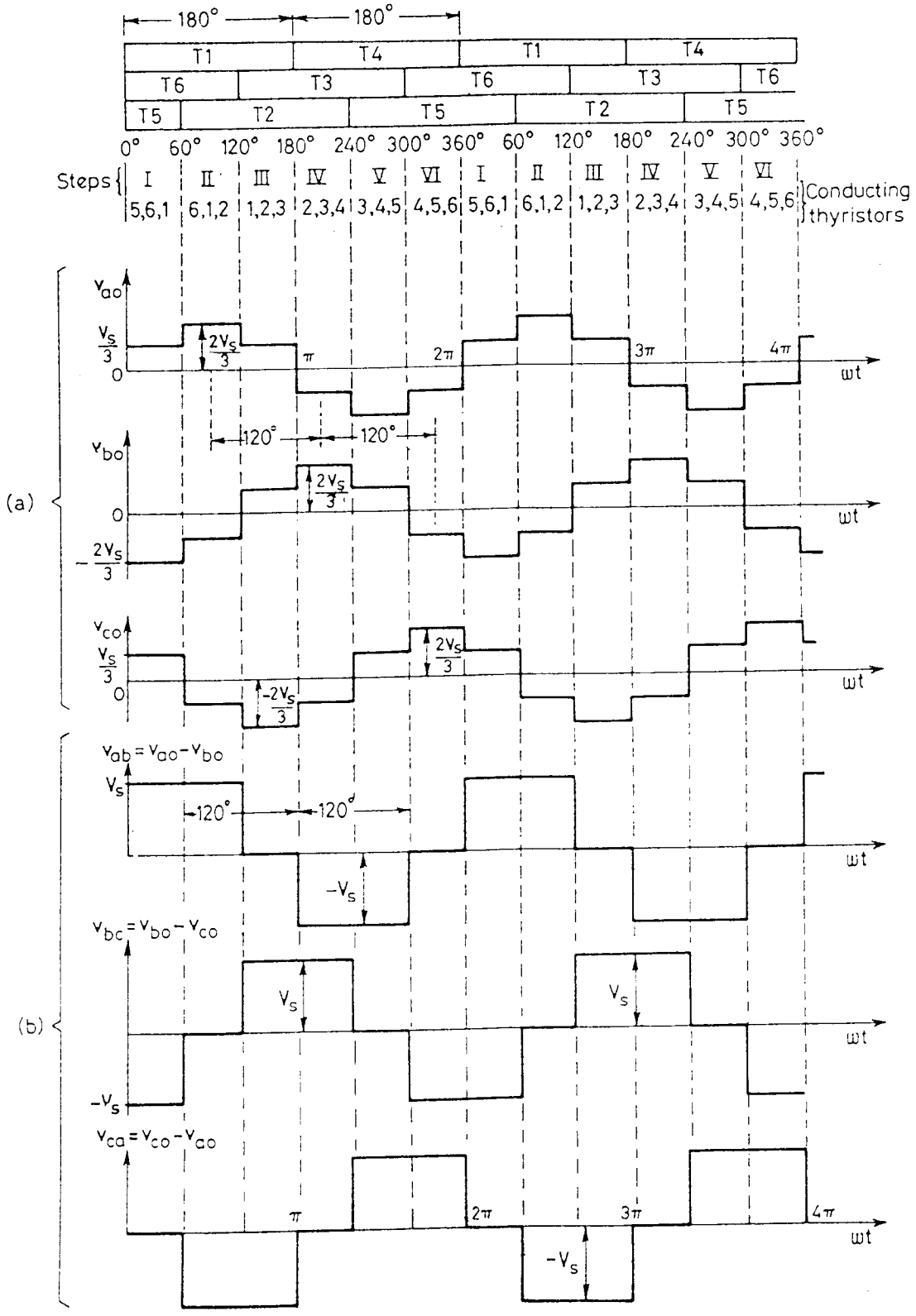


Fig. 8.20. Voltage waveforms for 180° mode 3-phase VSI.

It means that T1 conducts for 180° and T4 for the next 180° of a cycle. Thyristors in the upper group, *i.e.* T1, T3, T5 conduct at an interval of 120°. It implies that if T1 is fired at $\omega t = 0°$, then T3 must be fired at $\omega t = 120°$ and T5 at $\omega t = 240°$. Same is true for lower group of SCRs. On the basis of this firing scheme, a table is prepared as shown at the top of Fig. 8.20. In this table, first row shows that T1 from upper group conducts for 180°, T4 for the next 180° and then again T1 for 180° and so on. In the second row, T3 from the upper group is shown to start conducting 120°after T1 starts conducting. After T3 conduction for 180°, T6 conducts for the next 180° and again T3 for the next 180° and so on. Further, in the third row, T5 from the upper group starts conducting 120° after T3 or 240° after T1. After T5 conduction for 180°, T2 conducts for the next 180°, T5 for the next 180° and so on. In this manner, the pattern of firing the six SCRs is identified. This table shows that T5, T6, T1 should be gated for step I ; T6, T1, T2 for step II ; T1, T2, T3 for step III ; T2, T3, T4 for step IV and so on. Thus the sequence of firing the thyristors is T1, T2, T3, T4, T5, T6 ; T1, T2.... It is seen from the table that in every step of 60° duration, only three SCRs are conducting-one from upper group and two from the lower group or two from the upper group and one from the lower group.

The circuit models for step I-IV are shown in Fig. 8.21. During step I, thyristors 5, 6, 1 are conducting. These are shown as closed switches and non-conducting SCRs 2, 3, 4 as open switches in Fig. 8.21 (*a*). The load terminals *a* and *c* are connected to the positive bus of dc source whereas terminal *b* is connected to the negative bus of dc source, Fig. 8.21 (*a*). The load voltage is $v_{ab} = v_{cb} = V_s$ in magnitude. The magnitude of line to neutral voltage can be obtained as under :

During step I, $0 \le \omega t < \frac{\pi}{3}$, Fig. 8.21 (*a*), thyristors conducting 5, 6, 1.

Current, $$i_1 = \frac{V_s}{Z + \frac{Z}{2}} = \frac{2}{3} \cdot \frac{V_s}{Z}$$

The line to neutral voltages are

$$v_{ao} = v_{co} = i_1 \frac{Z}{2} = \frac{V_s}{3}$$

and $$v_{0b} = i_1 Z = \frac{2 V_s}{3}$$

The above line to neutral voltages may be written as $v_{a0} = v_{c0} = \frac{V_s}{3}$ and $v_{b0} = -\frac{2V_s}{3}$. These voltages are shown in Fig. 8.20 (*a*) during step I. For the next step II, the line to neutral voltages are as under :

During step II, $\frac{\pi}{3} \le \omega t < \frac{2\pi}{3}$, Fig. 8.21 (*b*), thyristor conducting 6, 1, 2.

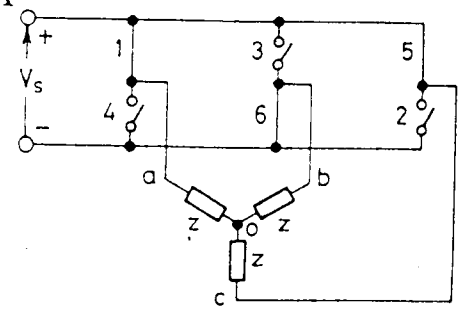
Current, $$i_2 = \frac{2}{3} \frac{V_s}{Z}$$

$\therefore$ $$v_{a0} = i_2 Z = \frac{2 V_s}{3} \; ; v_{0b} = v_{0c} = i_2 \frac{Z}{2} = \frac{V_s}{3}$$

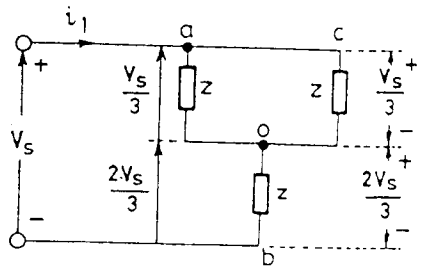
or $$v_{a0} = \frac{2V_s}{3}, \; v_{b0} = v_{c0} = -\frac{V_s}{3}.$$

These output voltages are plotted in Fig. 8.20 (*a*). In this manner, the variation of phase voltages v_{ao}, v_{bo}, v_{co} as obtained in Fig. 8.21 up to step IV and similarly for other steps, is plotted in Fig. 8.20 (*a*). It is clear that for each cycle of output voltage of each phase, six steps are required and each step has a duration of 60°.

Step I



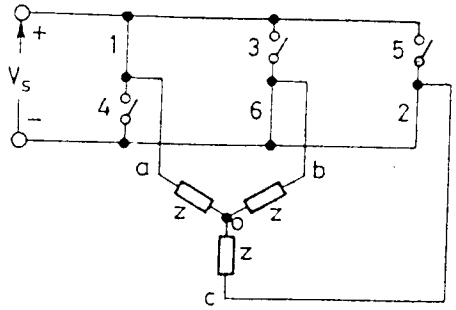
(*a*) 0—60° ; 5, 6, 1 closed.



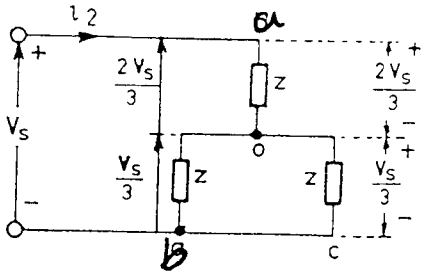
$v_{ao} = v_{co} = V_s/3$

$v_{bo} = -v_{ob} = -2V_s/3$

Step II



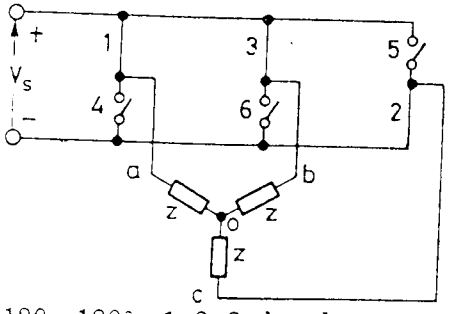
(*b*) 60—120° ; 6, 1,2 closed.



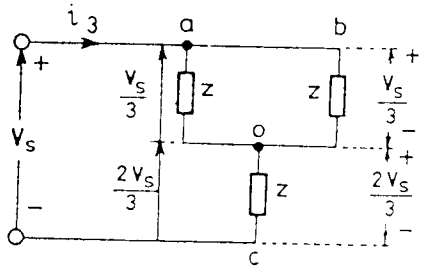
$v_{ao} = V_s/3$ × 2

$v_{bo} = v_{co} = -V_s/3$

Step III



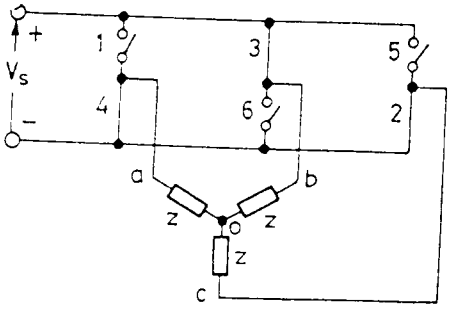
(*c*) 120—180° ; 1, 2, 3 closed.



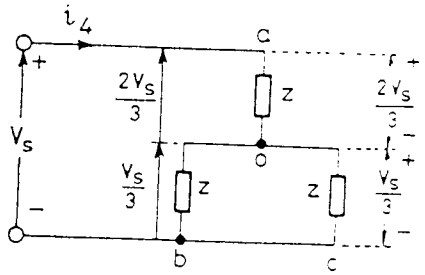
$v_{ao} = v_{bo} = V_s/3$

$v_{co} = -2V_s/3$

Step IV



(*d*) 180—240° ; 2, 3, 4 closed.



$v_{bo} = 2V_s/3$

$v_{ao} = v_{co} = -V_s/3$

Fig. 8.21. Equivalent circuits for a 3-phase six-step 180° mode inverter with a balanced star-connected load.

The line voltage $v_{ab} = v_{ao} + v_{ob}$ or $v_{ab} = v_{ao} - v_{bo}$ is obtained by reversing v_{bo} and adding it to v_{ao} as shown in Fig. 8.20 (*b*). Similarly, line voltages $v_{bc} = v_{bo} - v_{co}$ and $v_{ca} = v_{co} - v_{ao}$ are plotted in Fig. 8.20 (*b*).

The three rows in the top of Fig. 8.20 also indicate the pattern of gating signal waveforms. At $\omega t = \pi$, when i_{g1} is removed, T1 is turned off and simultaneously i_{g4} is applied to turn on T4. Similarly, at $\omega t = 2\pi/3$, when i_{g6} is cut off, T6 is turned off and at the same instant i_{g3} is applied to turn on T3. Same is true for other thyristors.

It is seen from Fig. 8.20 that phase voltages have six steps per cycle and line voltages have one positive pulse and one negative pulse (each of 120° duration) per cycle. The phase as well as line voltages are out of phase by 120°. The function of diodes D1 to D6 is to allow the flow of currents through them when the load is reactive in nature.

The three line output voltages can be described by the Fourier series as follows :

$$v_{ab} = \sum_{n = 1, 3, 5, \ldots}^{\infty} \frac{4V_s}{n\pi} \cos \frac{n\pi}{6} \sin n(\omega t + \pi/6) \qquad ...(8.44)$$

$$v_{bc} = \sum_{n = 1, 3, 5, \ldots}^{\infty} \frac{4V_s}{n\pi} \cos \frac{n\pi}{6} \sin n(\omega t - \pi/2) \qquad ...(8.45)$$

$$v_{ca} = \sum_{n = 1, 3, 5, \ldots}^{\infty} \frac{4V_s}{n\pi} \cos \frac{n\pi}{6} \sin n\left(\omega t + \frac{5\pi}{6}\right) \qquad ...(8.46)$$

For $n = 3$, $\cos \frac{3\pi}{6} = 0$. Thus, all triplen harmonics are absent from the line voltages as given by Eqs. (8.44) to (8.46).

The line voltage waveforms shown in Fig. 8.20 represent a balanced set of three-phase alternating voltages. During the six intervals, these voltages are well defined. Therefore, these voltages are independent of the nature of load circuit which may consist of any combination of resistance, inductance and capacitance and the load may be balanced or unbalanced, linear or nonlinear.

Fourier series expansion of line to neutral voltage v_{ao} in Fig. 8.20 is given by

$$v_{ao} = \sum_{n = 6k \pm 1}^{\infty} \frac{2V_s}{n\pi} \sin n\omega t \qquad ...(8.47)$$

where $k = 0, 1, 2, \ldots$

For a linear star-connected balanced load, phase or line currents can be obtained from Eq. (8.47). Expressions similar to Eq. (8.47) can be written for v_{bo} and v_{co} by replacing ωt by $(\omega t - 120°)$ and $(\omega t - 240°)$ respectively.

In Fig. 8.21, load is assumed star connected and three phase and line voltages are obtained as shown in Fig. 8.20. For a delta connected load also, phase or line voltage waveforms v_{ab}, v_{bc}, v_{ca} as shown in Fig. 8.20 would be obtained directly. Therefore, for a linear delta-connected load, phase and line currents can be obtained from Eqs. (8.44) to (8.46). From Eq. (8.44), rms value of nth component of line voltage is

$$V_{Ln} = \frac{4V_s}{\sqrt{2}\, n\pi} \cos \frac{n\pi}{6} \qquad ...(8.48)$$

Rms value of fundamental line voltage,

$$V_{L1} = \frac{4\,V_s}{\sqrt{2}\cdot\pi}\cos\frac{\pi}{6} = 0.7797\,V_s \qquad ...(8.49)$$

It is seen from line voltage waveform v_{ab} in Fig. 8.20 (a) that line voltage is V_s from 0° to 120°. Therefore, rms value of line voltage V_L is

$$V_L = \left[\frac{1}{\pi}\int_0^{2\pi/3} V_s^2\, d\,(\omega t)\right]^{1/2} = \sqrt{\frac{2}{3}}\,V_s = 0.8165\,V_s \qquad ...(8.50)$$

Rms value of phase voltage V_p is

$$V_p = \frac{V_L}{\sqrt{3}} = \frac{\sqrt{2}}{3}\,V_s = 0.4714\,V_s \qquad ...(8.51)$$

Rms value of fundamental phase voltage, from Eq. (8.47), is

$$V_{p1} = \frac{2V_s}{\sqrt{2}\,\pi} = 0.4502\,V_s = \frac{V_{L1}}{\sqrt{3}} \qquad ...(8.52)$$

8.4.2. Three-phase 120 Degree Mode VSI

The power circuit diagram of this inverter is the same as that shown in Fig. 8.19. For the 120-degree mode VSI, each thyristor conducts for 120° of a cycle. Like 180° mode, 120° mode inverter also requires six steps, each of 60° duration, for completing one cycle of the output ac voltage.

For this inverter too, a table giving the sequence of firing the six thyristors is prepared as shown in the top of Fig. 8.22. In this table, first rows shows that T1 conducts for 120° and for the next 60°, neither T1 nor T4 conducts. Now T4 is turned on at $\omega t = 180°$ and it further conducts for 120°, *i.e.* from $\omega t = 180°$ to $\omega t = 300°$. This means that for 60° interval from $\omega t = 120°$ to $\omega t = 180°$, series connected SCRs do not conduct. At $\omega t = 300°$, T4 is turned off, then 60° interval elapses before T1 is turned on again at $\omega t = 360°$. In the second row, T3 is turned on at $\omega t = 120°$ as in 180° mode inverter. Now T3 conducts for 120°, then 60° interval elapses during which neither T3 nor T6 conducts. At $\omega t = 300°$, T6 is turned on, it conducts for 120° and then 60° interval elapses after which T3 is turned on again. The third row is also completed similarly. This table shows that T6, T1 should be gated for step I ; T1, T2 for step II ; T2, T3 for step III and so on. The sequence of firing the six thyristors is the same as for the 180° mode inverter. During each step, only two thyristors conduct for this inverter — one from the upper group and one from the lower group ; but in 180° mode inverter, three thyristors conduct in each step.

The circuit models for steps I-IV are shown in Fig. 8.23, where load is assumed to be resistive and star connected. During step I, thyristors 6, 1 are conducting and as such load terminal a is connected to the positive bus of dc source whereas terminal b is connected to negative bus of dc source, Fig. 8.23 (a). Load terminal c is not connected to dc bus. The line to neutral voltages, from Fig. 8.23 (a) are

$$v_{ao} = \frac{V_s}{2}, \quad v_{ob} = \frac{V_s}{2}$$

or

$$v_{bo} = -\frac{V_s}{2}$$

and

$$v_{co} = 0$$

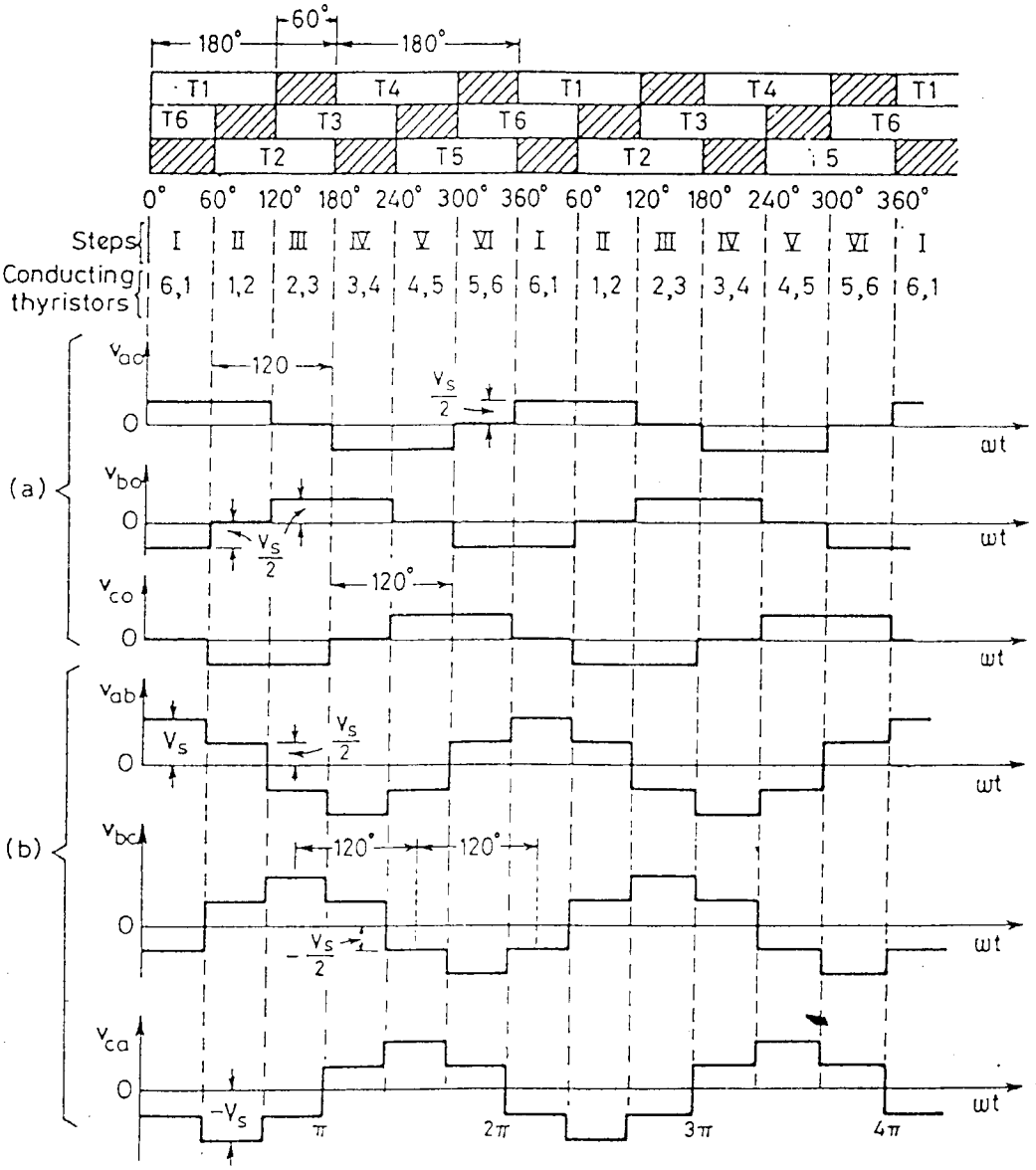


Fig. 8.22. Voltage waveforms for 120°mode six-step 3-phase VSI.

These voltages are shown in Fig. 8.22 (*a*) during step I of 0° – 60°. For step II, thyristor 1, 2 conduct and load voltages are $v_{ao} = V_s/2$, $v_{co} = -V_s/2$ and $v_{bo} = 0$, Fig. 8.23 (*b*) ; thes voltages are plotted in Fig. 8.22 (*a*). This procedure is followed for obtaining load voltages fc the remaining steps and these phase voltages are then plotted in Fig. 8.22 (*a*).

The line voltages $v_{ab} = v_{ao} - v_{bo}$

$v_{bc} = v_{bo} - v_{co}$

and $v_{ca} = v_{co} - v_{ao}$

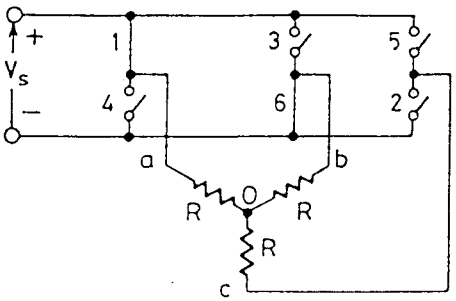
are also plotted in Fig. 8.19 (*b*).

It is seen from Fig. 8.22 that phase voltages have one positive pulse and one negativ pulse (each of 120° duration) for one cycle of output alternating voltage. The line voltages however, have six steps per cycle of output alternating voltage.

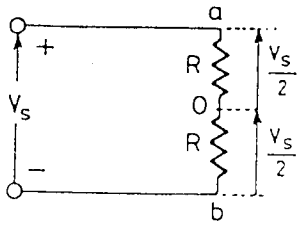
As stated before, the three rows in the top of Fig. 8.22 indicate the pattern of gating signa waveforms.

The merits and demerits of 120-degree mode inverter over 180-degree mode inverter ar as follows :

Step I



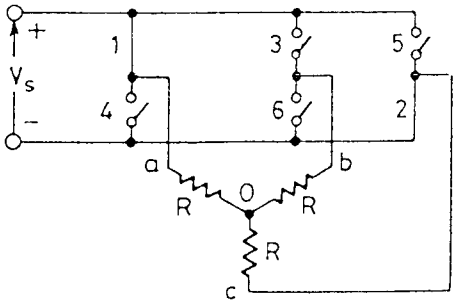
(*a*) 0—60° ; 6, 1 closed



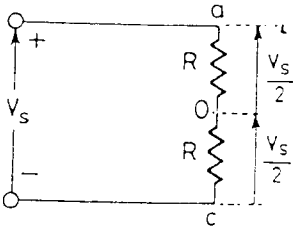
$v_{ao} = V_s/2$

$v_{bo} = -V_s/2$ and $v_{co} = 0$

Step II



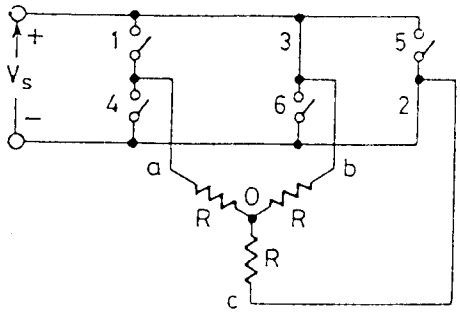
(*b*) 60—120° ; 1, 2 closed



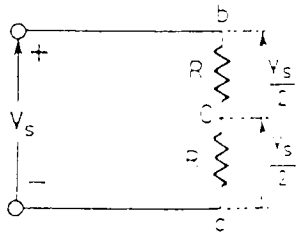
$v_{ao} = V_s/2$

$v_{co} = -V_s/2$ and $v_{bo} = 0$

Step III



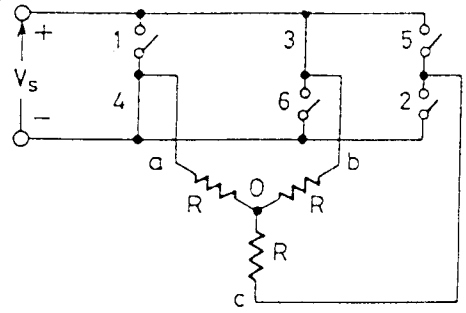
(*c*) 120—180° ; 2, 3 closed



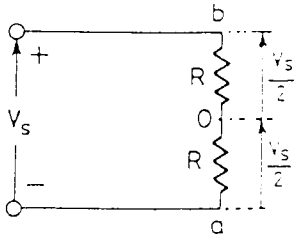
$v_{bo} = V_s/2$

$v_{co} = -V_s/2$ and $v_{ao} = 0$

Step IV



(*d*) 180—240° ; 3, 4 closed



$v_{bo} = V_s/2$

$v_{ao} = -V_s/2$ and $v_{co} = 0$

Fig. 8.23. Equivalent circuits for a 3-phase six-step 120° mode inverter with balanced star-connected resistive load.

(*i*) In the 180° mode inverter, when gate signal i_{g1} is cut-off to turn off T1 at $\omega t = 180°$, gating signal i_{g4} is simultaneously applied to turn on T4 in the same leg. In practice, a

commutation interval must exist between the removal of i_{g1} and application of i_{g4}, because otherwise dc source would experience a direct short-circuit through SCRs T1 and T4 in the same leg.

This difficulty is overcome considerably in 120-degree mode inverter. In this inverter, there is a 60° interval between the turning off of T1 and turning on of T4. During this 60° interval, T1 can be commutated safely. In general, this angular interval of 60° exists between the turning-off of one device and turning-on of the complementary device in the same leg. This 60° period provides sufficient time for the outgoing thyristor to regain forward blocking capability.

(*ii*) In the 120° mode inverter, the potentials of only two output terminals connected to the dc source are defined at any time of the cycle. The potential of the third terminal, pertaining to a particular leg in which neither device is conducting, is not well defined ; its potential therefore depends on the nature of the load circuit. Thus, the analysis of the performance of this inverter is complicated for a general load circuit. For a balanced resistive load, the potential of all the three terminals is, however, well defined. This is the reason load is assumed resistive in Fig. 8.23. For a balanced delta-connected resistive load, the line voltages as shown in Fig. 8.22 (*b*) are obtained directly.

The Fourier analysis of phase voltage waveform v_{ao} of Fig. 8.22 (*a*) is

$$v_{ao} = \sum_{n=1,3,5}^{\infty} \frac{2V_s}{n\pi} \cos\frac{n\pi}{6} \sin n(\omega t + \pi/6) \qquad ...(8.53)$$

Similarly,
$$v_{bo} = \sum_{n=1,3,5,.....}^{\infty} \frac{2V_s}{n\pi} \cos\frac{n\pi}{6} \sin n(\omega t - \pi/2) \qquad ...(8.54)$$

and
$$v_{co} = \sum_{n=1,3,5,.....}^{\infty} \frac{2V_s}{n\pi} \cos\frac{n\pi}{6} \sin n\left(\omega t + \frac{5\pi}{6}\right) \qquad ...(8.55)$$

The Fourier analysis of line voltage waveform v_{ab} of Fig. 8.22 (*b*) is

$$v_{ab} = \sum_{n=6k\pm1}^{\infty} \frac{3 \cdot V_s}{n\pi} \sin n\left(\omega t + \frac{\pi}{3}\right) \qquad ...(8.56)$$

where $k = 0, 1, 2, 3...$

Similar expressions for v_{bc} and v_{ca} can also be written.

Rms value of fundamental phase voltage, from Eq. (8.53), is

$$V_{p1} = \frac{2V_s}{\sqrt{2} \cdot \pi} \cdot \cos\frac{\pi}{6} = 0.3898\, V_s \qquad ...(8.57)$$

Rms value of phase voltage,

$$V_p = \left[\frac{1}{\pi}\int_0^{2\pi/3} \left(\frac{V_s}{2}\right)^2 \cdot d(\omega t)\right]^{1/2} = \sqrt{\frac{2}{3}} \cdot \frac{V_s}{2} = \frac{V_s}{\sqrt{6}} = 0.4082\, V_s \qquad ...(8.58)$$

Rms value of fundamental line voltage, from Eq. (8.56), is

$$V_{L1} = \frac{3V_s}{\sqrt{2} \cdot \pi} = 0.6752\, V_s = \sqrt{3}\, V_{p1} \qquad ...(8.59)$$

Rms value of line voltage,

$$V_L = \sqrt{3}\, V_p = \frac{V_s}{\sqrt{2}} = 0.7071\, V_s \qquad ...(8.60)$$

Example 8.8. *A three-phase bridge inverter delivers power to a resistive load from a 450 V dc source. For a star-connected load of 10 Ω per phase, determine for both (a) 180° mode and (b) 120° mode,*

(i) rms value of load current

(ii) rms value of thyristor current

(iii) load power.

Solution. For a resistive load, the waveform of load current is the same as that of the applied voltage. In view of this, waveforms of phase-load current and thyristor current are as shown in Fig. 8.24 (*a*) for 180° mode operation and in Fig. 8.24 (*b*) for 120° mode operation.

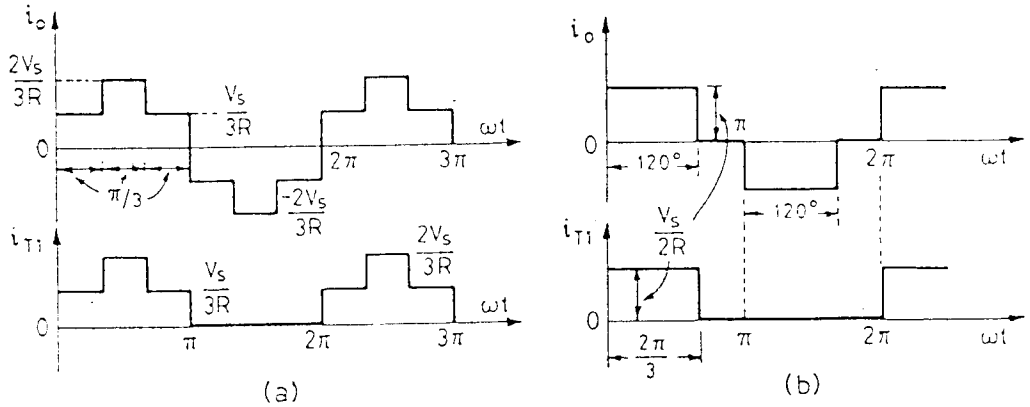


Fig. 8.24. Pertaining to example 8.8 (*a*) 180° mode (*b*) 120° mode.

(*a*) **180° mode** : Upper waveform of Fig. 8.24 (*a*) shows that rms value of per-phase load current I_{or} is given by

$$I_{or} = \left[\frac{1}{\pi}\left\{\left(\frac{V_s}{3R}\right)^2 \frac{\pi}{3} + \left(\frac{2V_s}{3R}\right)^2 \times \frac{\pi}{3} + \left(\frac{V_s}{3R}\right)^2 \frac{\pi}{3}\right\}\right]^{1/2}$$

$$= \left[\left(\frac{450}{3\times 10}\right)^2 \times \frac{2}{3} + \left(\frac{2\times 450}{3\times 10}\right)^2 \times \frac{1}{3}\right]^{1/2} = \sqrt{350} = 18.708 \text{ A}$$

Rms value of thyristor current is

$$I_{T1} = \left[\frac{1}{2\pi}\left\{\left(\frac{450}{3\times 10}\right)^2 \times \frac{2\pi}{3} + \left(\frac{2\times 450}{3\times 10}\right)^2 \times \frac{\pi}{3}\right\}\right]^{1/2}$$

$$= \sqrt{175} = 13.229 \text{ A}$$

Power delivered to load

$$= 3\, I_{or}^2\, R = 3\,(\sqrt{350})^2 \times 10 = 10.5 \text{ kW}$$

(*b*) **120° mode :** Upper waveform in Fig. 8.24 (*b*) gives rms value of per-phase load current I_{or} as under :

$$I_{or} = \left[\frac{1}{\pi}\left(\frac{450}{2\times 10}\right)^2 \times \frac{2\pi}{3}\right]^{1/2} = \sqrt{337.5} = 18.371 \text{ A}$$

Rms value of thyristor current.

$$I_{T1} = \left[\frac{1}{2\pi}\left(\frac{450}{2\times 10}\right)^2 \cdot \frac{2\pi}{3}\right]^{\frac{1}{2}} = 12.99\text{ A}$$

Load power $= 3 I_{T1}^2 R = 3 \times 337.5^2 \times 10 = 10.125\text{ kW}$

8.5. VOLTAGE CONTROL IN SINGLE-PHASE INVERTERS

AC loads may require constant or adjustable voltage at their input terminals. When such loads are fed by inverters, it is essential that output voltage of the inverters is so controlled as to fulfil the requirement of ac loads. Examples of such requirements are as under :

(*i*) An ac load may require a constant input voltage though at different levels. For such a load, any variations in the dc input voltage must be suitably compensated in order to maintain a constant voltage at the ac load terminals at a desired level.

(*ii*) In case inverter supplies power to a magnetic circuit, such as an induction motor, the voltage to frequency ratio at the inverter output terminals must be kept constant. This avoids saturation in the magnetic circuit of the device fed by the inverter.

The various methods for the control of output voltage of inverters are as under :

(*a*) External control of ac output voltage

(*b*) External control of dc input voltage

(*c*) Internal control of inverter.

The first two methods require the use of peripheral components whereas the third method requires no peripheral components. These methods are now briefly discussed.

8.5.1. External Control of ac Output Voltage

There are two possible methods of external control of ac output voltage obtained from inverter output terminals. These methods are :

(*a*) AC voltage control

(*b*) Series-inverter control

These are now discussed briefly.

(*a*) **AC voltage control** : In this method, an ac voltage controller is inserted between the output terminals of inverter and the load terminals as shown in Fig. 8.25. The voltage input to the ac load is regulated through the firing angle control of ac voltage controller. This method gives rise to higher harmonic content in the output voltage ; particularly when the output voltage from the ac voltage controller is at low level. This method is, therefore, rarely employed except for low power applications.

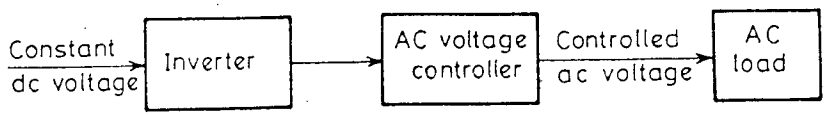


Fig. 8.25. External control of ac output voltage.

(*b*) **Series-inverter control** : This method of voltage control involves the use of two or more inverters in series. Fig. 8.26 (*a*) illustrates how the output voltage of two inverters can be summed up with the help of transformers to obtain an adjustable output voltage. In this figure, the inverter output is fed to two transformers whose secondaries are connected in series. Phasor sum of the two fundamental voltages V_{01}, V_{02} gives the resultant fundamental voltage V_0 as shown in Fig. 8.26 (*b*). Here V_0 is given by

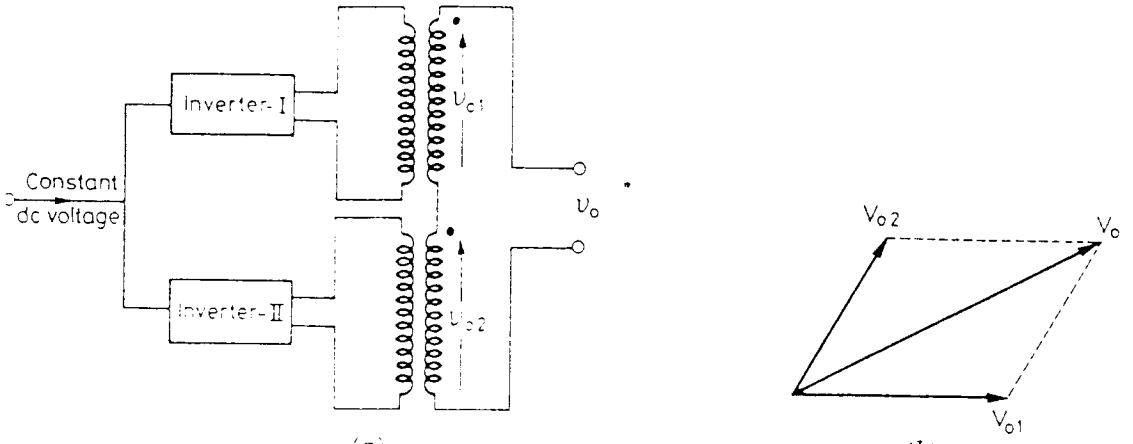


Fig. 8.26. Series inverter control of two inverters.

It is essential that the frequency of output voltages V_{01}, V_{02} from the two inverters is the same. When θ is zero, $V_0 = V_{01} + V_{02}$ and for $\theta = \pi$, $V_0 = 0$ in case $V_{01} = V_{02}$. The angle θ can be varied by the firing angle control of two inverters. The series connection of inverters, called *multiple converter control*, does not augment the harmonic content even at low output voltage levels.

8.5.2. External Control of dc Input Voltage

In case the available voltage source is ac, then dc voltage input to the inverter is controlled through a fully-controlled rectifier, Fig. 8.27 (*a*) ; through an uncontrolled rectifier and a chopper, Fig. 8.27 (*b*) ; or through an ac voltage controller and an uncontrolled rectifier, Fig. 8.27 (*c*). If available voltage is dc, then dc voltage input to the inverter is controlled by means of a chopper as shown in Fig. 8.27 (*d*).

Input voltage-control techniques shown in Fig. 8.27, in which dc voltage input to inverter is controlled by means of components external to the inverter, has the following main advantage.

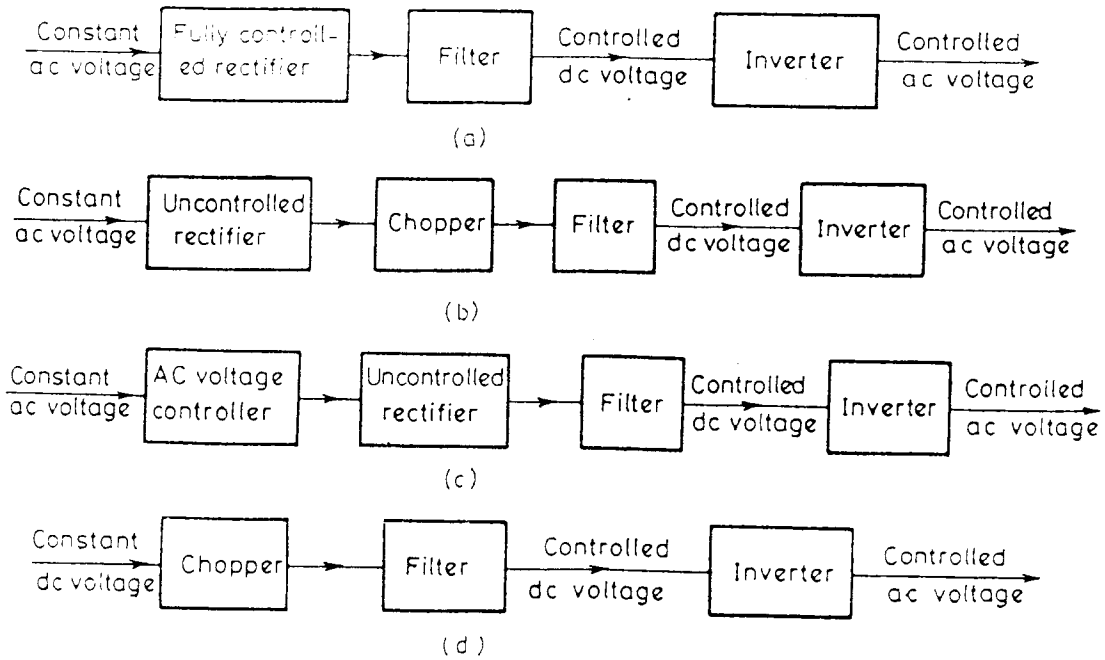


Fig. 8.27. External control of dc input voltage to inverter ; (*a*), (*b*) and (*c*) with ac source on the input (*b*) with dc source on the input.

(*i*) Output voltage waveform and its harmonic content are not affected appreciably as the inverter output voltage is controlled through the adjustment of dc input voltage to the inverter.

This method of voltage control, however, suffers from the following disadvantages :

(*i*) The number of power converters used for the control of inverter output voltage varies from two to three, Fig. 8.27. More power-handling stages result in more losses and reduced efficiency of the entire scheme.

(*ii*) For reducing the ripple content of dc voltage input to the inverter, filter circuit is required in all types of schemes shown in Fig. 8.27. Filter circuit increases the cost, weight and size and at the same time reduces efficiency and makes the transient response sluggish.

(*iii*) As the dc input is decreased, the commutating capacitor voltage also decreases. This has the effect of reducing the circuit turn-off time $\left(t = C\frac{V}{I}\right)$ for the SCR for a constant load current. Therefore, for a large variation of output voltage for a constant load current, control of dc input voltage is not conducive. This difficulty can, however, be overcome by a separate fixed dc source for charging the commutating capacitor, but this makes the scheme costly and complicated.

8.5.3. Internal Control of Inverter

Output voltage from an inverter can also be adjusted by exercising a control within the inverter itself. The most efficient method of doing this is by pulse-width modulation control used within an inverter. This is discussed briefly in what follows.

Pulse width modulation control. In this method, a fixed dc input voltage is given to the inverter and a controlled ac output voltage is obtained by adjusting the on and off periods of the inverter components. This is the most popular method of controlling the output voltage and this method is termed as *pulse–width modulation* (PWM) control.

The advantages possessed by PWM technique are as under :

(*i*) The output voltage control with this method can be obtained without any additional components.

(*ii*) With this method, lower order harmonic can be eliminated or minimised along with its output voltage control. As higher order harmonics can be filtered easily, the filtering requirements are minimised.

The main disadvantage of this method is that the SCRs are expensive as they must possess low turn-on and turn-off times.

PWM inverters are quite popular in industrial applications, these are therefore discussed in detail in the next section.

8.6. PULSE-WIDTH MODULATED INVERTERS

PWM inverters are gradually taking over other types of inverters in industrial applications. PWM techniques are characterised by constant amplitude pulses. The width of these pulses is, however, modulated to obtain inverter output voltage control and to reduce its harmonic content. Different PWM techniques are as under :

(*a*) Single-pulse modulation (*b*) Multiple-pulse modulation

(*c*) Sinusoidal-pulse modulation.

In PWM inverters, forced commutation is essential. The three PWM techniques listed above differ from each other in the harmonic content in their respective output voltages. Thus, choice of a particular PWM technique depends upon the permissible harmonic content

PWM inverter is supplied from a diode bridge rectifier and an ... the inverter topology remains the same as in Fig. 8.2 (*a*) for a single-phase inverter and in Fig. 8.19 for a three-phase inverter. But now the devices are switched on and off several times within each half cycle to control the output voltage which has low harmonic content.

In the following lines, the basic principles of PWM techniques for single-phase inverters are illustrated and then the methods of obtaining such output voltages are considered.

8.6.1. Single-pulse Modulation

The output voltage from single-phase full-bridge inverter is shown in Fig. 8.28 (*a*). When this waveform is modulated, the output voltage is of the form shown in Fig. 8.28 (*b*). It consists of a pulse of width $2d$ located symmetrically about $\pi/2$ and another pulse located symmetrically about $3\pi/2$. The range of pulse width $2d$ varies from 0 to π ; *i.e.* $0 < 2d < \pi$. The output voltage is controlled by varying the pulse-width $2d$. This shape of the output voltage wave shown in Fig. 8.28 (*b*) is called quasi-square wave.

Fourier analysis of Fig. 8.28 (*b*) is as under :

$$A_n = \frac{2}{\pi}\int_{(\pi/2-d)}^{(\pi/2+d)} V_s \sin n\omega t \cdot d(\omega t) = \frac{4V_s}{n\pi}\left[\sin\frac{n\pi}{2}\sin nd\right] \qquad ...(8.61)$$

Positive and negative half cycles of v_0 in Fig. 8.28 (*b*) are symmetrical about $\pi/2$ and $3\pi/2$ respectively. In addition, these half cycles are also identical. As a result, coefficient $B_n = 0$. Thus the waveform of Fig. 8.28 (*b*) can be described by Fourier series as

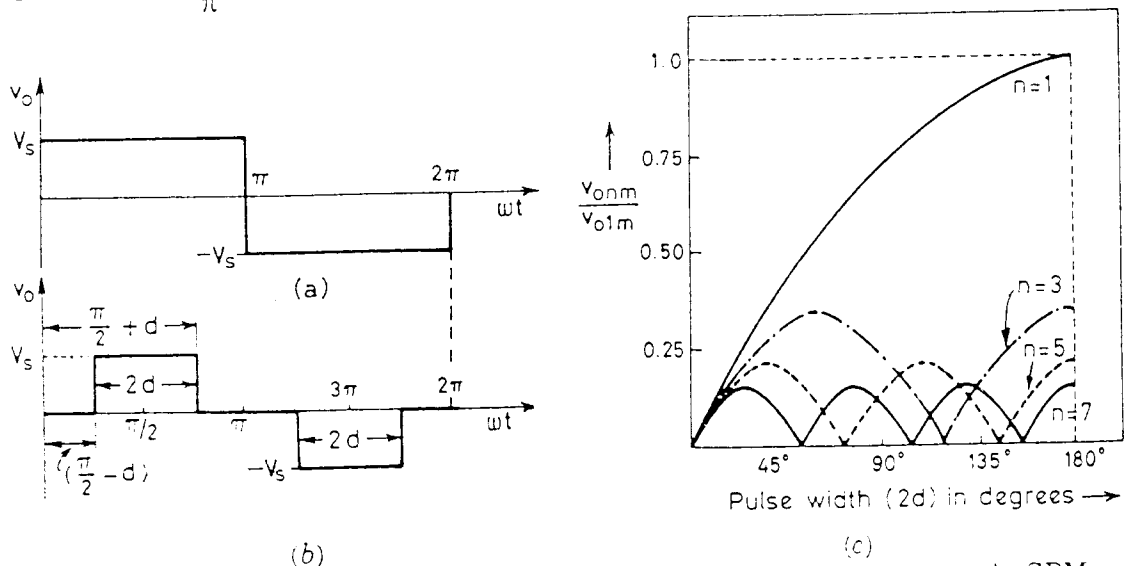
$$v_0 = \sum_{n=1,3,5}^{\infty} \frac{4V_s}{n\pi}\sin\frac{n\pi}{2}\sin nd\sin n\omega t \qquad ...(8.62)$$

or
$$v_0 = \frac{4V_s}{\pi}\left[\sin d\sin\omega t - \frac{1}{3}\sin 3d\sin 3\omega t + \frac{1}{5}\sin 5d\sin 5\omega t.....\right] \qquad ...(8.63)$$

When pulse width $2d$ is equal to its maximum value of π radians, then the fundamental component of output voltage, from Eq. (8.63), has a peak value of

$$v_{01m} = \frac{4V_s}{\pi} \qquad ...(8.64)$$

For pulse width other than $2d = \pi$ radians, the peak value of fundamental component, from Eq. (8.63), is $\frac{4V_s}{\pi}\sin d$.



(*b*) (*c*)

Fig. 8.28. (*a*), (*b*) Single-pulse modulation (SMP) (*c*) Harmonic content in SPM.

If nd is made equal to π or $d = \frac{\pi}{n}$ or if pulse width is made equal to $2d = \frac{2\pi}{n}$, Eq. (8.62) shows that nth harmonic is eliminated from the inverter output voltage. For example, for eliminating third harmonic, pulse width of $2d$ must be equal to 120°.

The peak value of nth harmonic, from Eq. (8.62), is

$$v_{onm} = \frac{4\,V_s}{n\pi} \sin nd \qquad ...(8.65)$$

From Eqs. (8.64) and (8.65), $$\frac{v_{onm}}{v_{01m}} = \frac{\sin nd}{n} \qquad ...(8.66)$$

In Eq. (8.66), note that v_{01m} is the peak value of the fundamental component of rectangular voltage wavefrom of width $2d = \pi$. The ratio as given by Eq. (8.66) is plotted in Fig. 8.28 (*c*) for $n = 1$ (plot of $\sin d$), $n = 3$ (plot of $\sin 3d/3$), $n = 5, 7$ for different pulse widths. It is seen from these curves that when fundamental component is reduced to 0.5 for $2d = 60°$, the amplitude of third harmonic is $\frac{1}{3} \sin 90 = 0.33$. When fundamental component is reduced to about 0.143, all the three harmonics (3, 5, 7) become almost comparable to the fundamental. This shows that in this method of voltage control, a great deal of harmonic content is introduced in the output voltage, particularly at low output voltage levels.

The rms value of output voltage, from Fig. 8.28 (*b*), is

$$V_{or} = \left[\frac{V_s^2 \cdot 2d}{\pi}\right]^{1/2} = V_s \left[\frac{2d}{\pi}\right]^{1/2} \qquad ...(8.67)$$

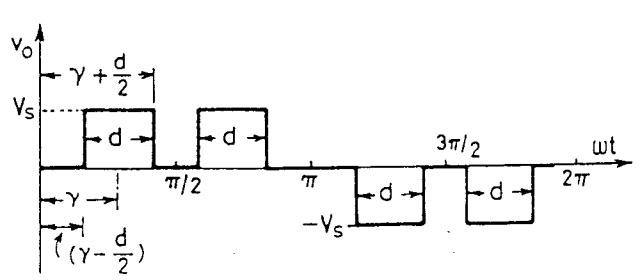
8.6.2. Multiple-pulse Modulation

This method of pulse modulation is an extension of single-pulse modulation. In multiple-pulse modulation (MPM), several equidistant pulses per half cycle are used. For simplicity, the effect of using two symmetrically spaced pulses per half cycle, Fig. 8.29 (*a*), is investigated here. In this figure, pulse width is taken half of that in Fig. 8.28 (*b*), but their amplitudes are the same. This means that rms values of pulses in Figs. 8.28 (*b*) and 8.29 (*a*) are equal to that given in Eq. (8.67). For the waveform of Fig. 8.29 (*a*), Fourier constants are as under :

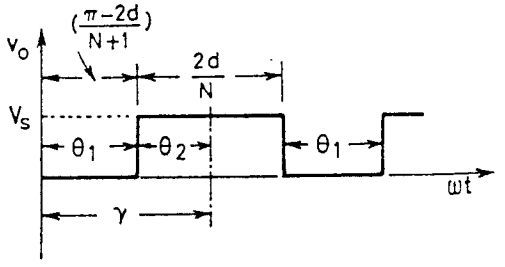
$$A_n = \frac{2}{\pi} \int_0^{\pi} v_0 \sin n\omega t \cdot d(\omega t)$$

$$= \frac{2}{\pi} \int_{(\gamma - d/2)}^{(\gamma + d/2)} V_s \cdot \sin n\omega t \cdot d(\omega t) \cdot 2$$

The use of factor 2 in the above expression accounts for the two pulses from 0 to π in Fig. 8.29 (*a*)



(*a*)



(*b*)

$$A_n = \frac{4\,V_s}{n\,\pi}\left|\cos n\,\omega t\right|_{\gamma+d/2}^{\gamma-d/2} = \frac{8V_s}{n\pi}\sin n\gamma \sin\frac{nd}{2} \qquad ...(8.68)$$

As in Fig. 8.28 (*b*), $B_n = 0$ in Fig. 8.29 (*a*) also.

Therefore, the waveform of Fig. 8.29 (*a*) can be described by Fourier series as

$$v_0 = \sum_{n=1,3,5}^{\infty} \frac{8\,V_s}{n\pi}\sin n\gamma \sin\frac{nd}{2}\sin n\omega t \qquad ...(8.69)$$

or
$$v_0 = \frac{8\,V_s}{\pi}\left[\sin\gamma\sin\frac{d}{2}\sin\omega t + \frac{1}{3}\sin 3\gamma\cdot\sin\frac{3d}{2}\sin 3\,\omega t + \frac{1}{5}\sin 5\gamma\sin\frac{5d}{2}\sin 5\omega t + \ldots\right] \qquad ...(8.70)$$

The amplitude of the nth harmonic of the two-pulse waveform of Fig. 8.29 (*a*), from Eq. (8.69), is

$$v_n = \frac{8\,V_s}{n\pi}\sin n\gamma\cdot\sin\frac{nd}{2} \qquad ...(8.71)$$

Eq. (8.71) shows that magnitude of v_n depends upon γ and d. This expression also shows that when $\gamma = \frac{\pi}{n}$ or $d = \frac{2\pi}{n}$, nth harmonic can be eliminated from the output voltage. But this has the effect of reducing the fundamental component of output voltage. For example, take pulse width $2d = 72°$ for single-pulse modulation of Fig. 8.28 (*b*). Then, from Eq. (8.65), the peak value of fundamental voltage component is

$$v_{01m} = \frac{4\,V_s}{\pi}\sin 36° = 0.7484\,V_s.$$

For two-pulse modulation and pulse width $d = 36°$. γ in Fig. 8.29 (*a*), is

$$\gamma = \frac{180-72}{3} + \frac{72}{4} = 54°$$

or in general.
$$\gamma = \frac{\pi - 2d}{N+1} + \frac{d}{N} \qquad ...(8.72)$$

Eq. (8.72) is valid in case pulses of equal width are symmetrically spaced. Here N is the number of pulses per half cycle.

Eq. (8.72) can also be obtained by referring to Fig. 8.29 (*b*). For N pulses per half cycle, there are $(N+1)$ intervening equidistant spaces, each of width θ_1 as shown in Fig. 8.29 (*b*). Note that for these equidistant spaces, $v_0 = 0$. Total width of these $(N+1)$ equidistant spaces $= (N+1)\,\theta_1 = (\pi - \text{width of } N \text{ pulses}) = (\pi - 2d)$

or
$$\theta_1 = \frac{\pi - 2d}{N+1}$$

Fig. 8.29 (*b*) shows that $\theta_2 = \text{half of the pulse width} = \frac{d}{N}$. This figure also reveals that

$$\gamma = \theta_1 + \theta_2$$

or
$$\gamma = \frac{\pi - 2d}{N+1} + \frac{d}{N} \qquad ...(8.72)$$

Peak value of fundamental voltage component, from Eq. (8.71), is

$$v_{01m} = \frac{8\,V_s}{\pi}\sin 54\sin 18° = 0.637\,V_s.$$

It is seen from above that fundamental component of output voltage is lower (0.637 V_s) for two-pulse modulation than it is for single-pulse modulation (0.7484 V_s). It can be shown that for a larger value of pulses per half cycle, the amplitudes of lower order harmonics are reduced but those of some higher harmonics are increased significantly. But this is no disadvantage as higher order harmonics can be filtered out easily.

The symmetrical modulated wave shown in Fig. 8.29 (*a*) can be generated by comparing an adjustable square voltage wave V_r of frequency ω with a triangular carrier wave V_c of frequency ω_c as shown in Fig. 8.30 (*b*). This comparison is done in a comparator, Fig. 8.30 (*a*). In Fig. 8.29 (*a*), there are only two pulses per half-cycle but in Fig. 8.30 (*b*), there are

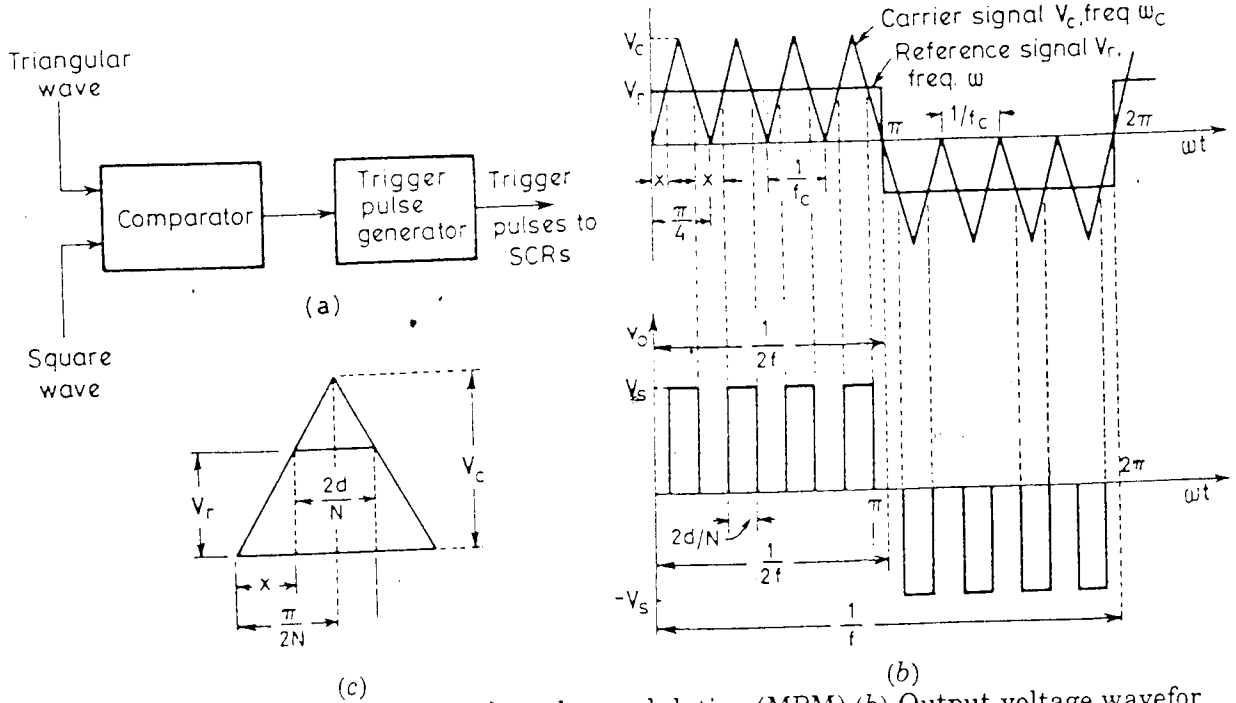


Fig. 8.30. (*a*) Pertaining to multiple-pulse modulation (MPM) (*b*) Output voltage wavefor with MPM (*c*) V_c and V_r shown on a larger scale.

four pulses per half cycle. The triggering pulses for thyristors are generated at the points of intersection of the carrier and reference signal waves. The firing pulses so generated turn-on the SCRs so that output voltage v_0 is available during the interval triangular voltage wave exceeds the square modulating wave shown in Fig. 8.30 (*b*). In this figure, f_c and f are the frequencies in Hz for the carrier signal and reference signal respectively. This figure reveals that $\frac{1}{f_c} = \frac{\pi}{4}$ and $\frac{1}{2f} = \pi$ and the number of trigger pulses is $\frac{4}{\pi} \times \frac{\pi}{1} = 4$. In general, the number of pulses generated per half cycle can be determined from Fig. 8.30 (*b*) as under :

For triangular carrier wave, pulse width $= \frac{1}{f_c}$.

For square reference wave, width of half-cycle $= \frac{1}{2f}$.

$\therefore$ Number of pulses per half-cycle

= Number of hill-tops per half-cycle

Length of half-cycle of square reference wave

or $$N = \frac{1/2f}{1/f_c} = \frac{f_c}{2f} = \frac{\omega_c}{2\omega} \qquad ...(8.73)$$

Note that N in Eq. (8.73) must be an integer. The pulse height of the reference, or modulating, signal can be controlled within the range $0 < V_r < V_c$ and pulse width $\frac{2d}{N}$ varied in the range $0 < \frac{2d}{N} < \frac{\pi}{N}$ by adjusting the magnitude V_r of the reference square wave. The pulse width is $2d/N$ on the assumption of same rms voltage as in single-pulse modulation.

In Fig. 8.30 (b), pulse width $2d/N$ is given by

$$\frac{2d}{N} = \left(\frac{\pi}{4} - 2x\right)$$

A general expression for the pulse width can be obtained by sketching the first cycle of carrier signal on a larger scale as in Fig. 8.30 (c). From this figure, pulse width, in general, is given by

$$\frac{2d}{N} = \left(\frac{\pi}{4} - 2x\right) \qquad ...(8.74)$$

where x, defined in Fig. 8.30 (c), is

$$\frac{V_c}{\pi/2N} = \frac{V_r}{x}$$

or $$x = \frac{\pi}{2N} \cdot \frac{V_r}{V_c}$$

From Eq. (8.74), the pulse width is

$$\frac{2d}{N} = \left(\frac{\pi}{N} - \frac{\pi}{N} \cdot \frac{V_r}{V_c}\right) = \left(1 - \frac{V_r}{V_c}\right)\frac{\pi}{N} \qquad ...(8.75)$$

In MPM method, lower order harmonics can be eliminated by a proper choice of $2d$ and γ. But the rms voltage in Figs. 8.28 to 8.30 is the same, *i.e.*

$$V_{or} = V_s\left[\frac{2d}{\pi}\right]^{1/2}$$

This means that if lower order harmonics are eliminated, the magnitude of higher order harmonics would go up. But this is not a disadvantage, as higher order harmonics can be filtered out by the use of filters at the output terminals of the inverters.

8.6.3. Sinusoidal-pulse Modulation (sin M)

In this method of modulation, several pulses per half cycle are used as in the case of multiple-pulse modulation (MPM). In MPM, the pulse width is equal for all the pulses. But is sin M, the pulse width is a sinusoidal function of the angular position of the pulse in a cycle as shown in Fig. 8.31.

For realizing sin M, a high-frequency triangular carrier wave v_c is compared with a sinusoidal reference wave v_r of the desired frequency. The intersection of v_c and v_r waves determines the switching instants and commutation of the modulated pulse. In Fig. 8.31, V_c is the peak value of triangular carrier wave and V_r that of the reference, or modulating, signal.

The carrier and reference waves are mixed in a comparator. When sinusoidal wave has magnitude higher than the triangular wave, the comparator output is high, otherwise it is

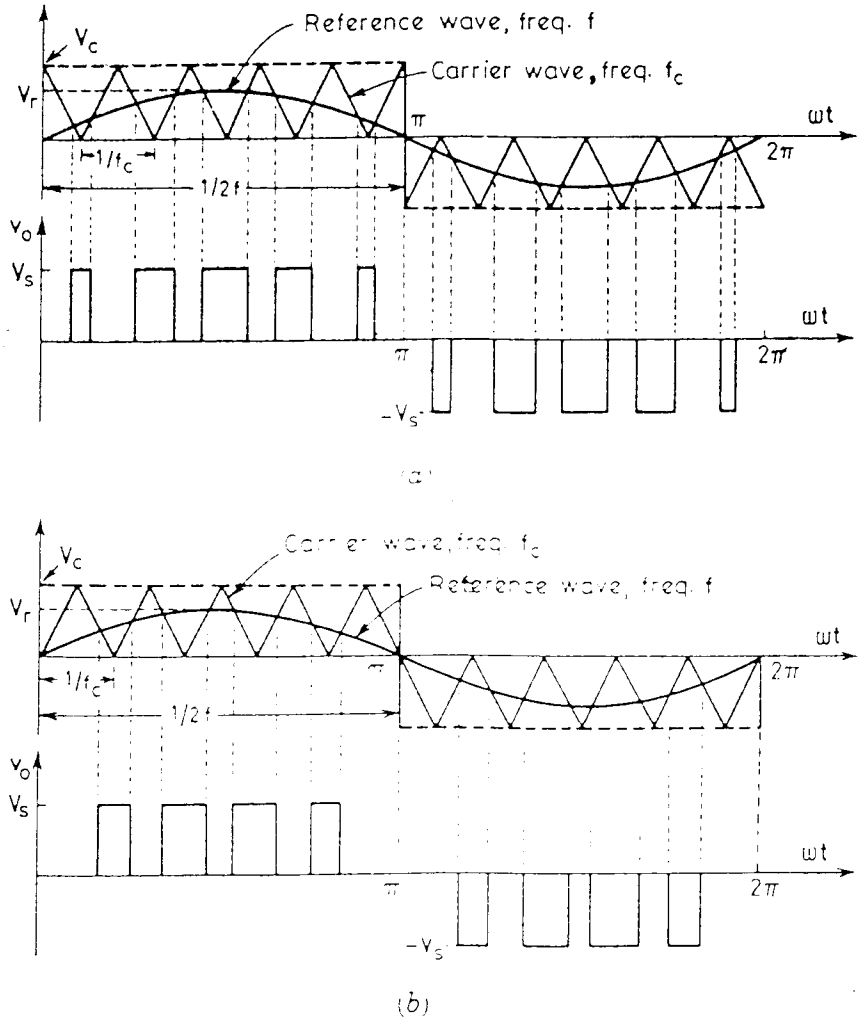


Fig. 8.31. Output voltage waveforms with sinusoidal pulse modulation.

low. The comparator output is processed in a trigger pulse generator in such a manner that the output voltage wave of the inverter has a pulse width in agreement with the comparator output pulse width.

When triangular carrier wave has its peak coincident with zero of the reference sinusoid, there are $N = \frac{f_c}{2f}$ pulses per half cycle ; Fig. 8.31 (a) has five pulses. In case zero of the triangular wave coincides with zero of the reference sinusoid, there are $(N - 1)$ pulses per half cycle ; Fig. 8.31 (b) has $\left(\frac{f_c}{2f} - 1\right)$, *i.e.* four, pulses per cycle.

The ratio of V_r/V_c is called the *modulation index* (MI) and it controls the harmonic content of the output voltage waveform. The magnitude of fundamental component of output voltage is proportional to MI, but MI can never be more than unity. Thus the output voltage is controlled by varying MI.

Harmonic analysis of the output modulated voltage wave reveals that sin M has the following important features :

(i) For MI less than one, largest harmonic amplitudes in the output voltage are associated with harmonics of order $f_c/f \pm 1$ or $2N \pm 1$, where N is the number of pulses per half cycle.

frequency can be raised, which can then be filtered out easily. In Fig. 8.31 (a), $N = 5$, therefore harmonics of order 9 and 11 become significant in the output voltage. It may be noted that the highest order of significant harmonic of a modulated voltage wave is centred around the carrier frequency f_c [in Fig. 8.31 (a), $f_c = 10$].

It is observed from above that as N is increased, the order of significant harmonic increases and the filtering requirements are accordingly minimised. But higher value of N entails higher switching frequency of thyristors. This amounts to more switching losses and therefore an impaired inverter efficiency. Thus a compromise between the filtering requirements and inverter efficiency should be made.

(ii) For MI greater than one, lower order harmonics appear, since for $MI > 1$, pulse width is no longer a sinusoidal function of the angular position of the pulse.

In addition to the three PWM techniques discussed above, there is another PWM technique called multiple-pulse modulation with selective reduction (MPMSR). In this technique, the number of M pulse positions in each quarter cycle are so selected as to reduce or eliminate M harmonics from the output voltage waveform [6]. This PWM technique will, however, not be discussed here.

8.6.4. Realization of PWM in Single-phase Bridge Inverters

The output voltage waveforms shown in Figs. 8.28 to 8.31 reveal that output voltage from an inverter is V_s, zero or $-V_s$. Such waveforms can be realized in single-phase inverters as under :

(a) **Single-phase full-bridge inverter**. In the inverter of Fig. 8.2 (a), when $+V_s$ is to be obtained in the positive half cycle, thyristors T1, T2 are turned on. For obtaining $-V_s$ in the negative half cycle, thyristors T3, T4 should be turned on. For zero output voltage, *i.e.* if the load is to be short-circuited ; then T1, D3 or T3, D1 from positive group ; or T4, D2 or T2, D4 from negative group should conduct depending upon the direction of load current. This means that for obtaining zero output voltage at the end of each pulse, one of the two conducting SCRs should only be turned off. Under this strategy, only one thyristor need be turned on for obtaining the next voltage pulse. Switching on and commutation of thyristors should be so arranged as to utilize the thyristors symmetrically. Let us illustrate this with an example.

Suppose output voltage of pulse width $2\pi/3$ radians is to be obtained in each half cycle. This pulse width is symmetrically placed as shown in Fig. 8.32. The waveform of load current

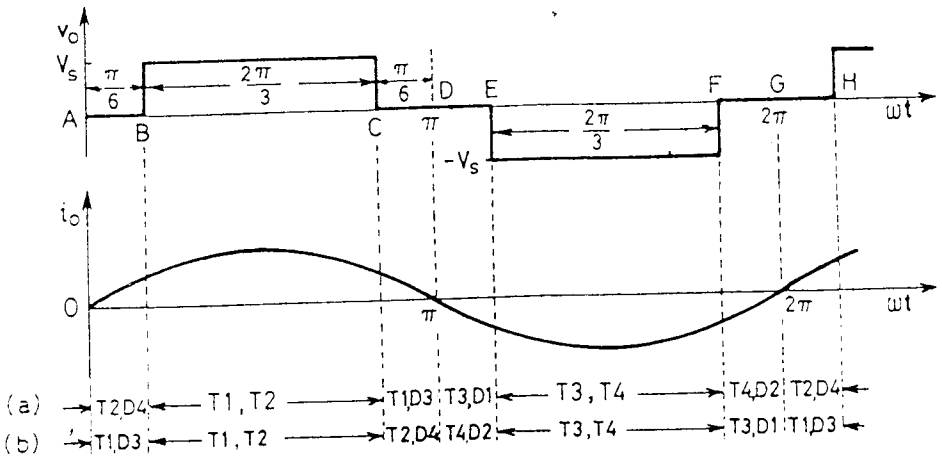


Fig. 8.32. Conduction of various components for single-phase bridge inverter of Fig. 8.2 (a).

NINE

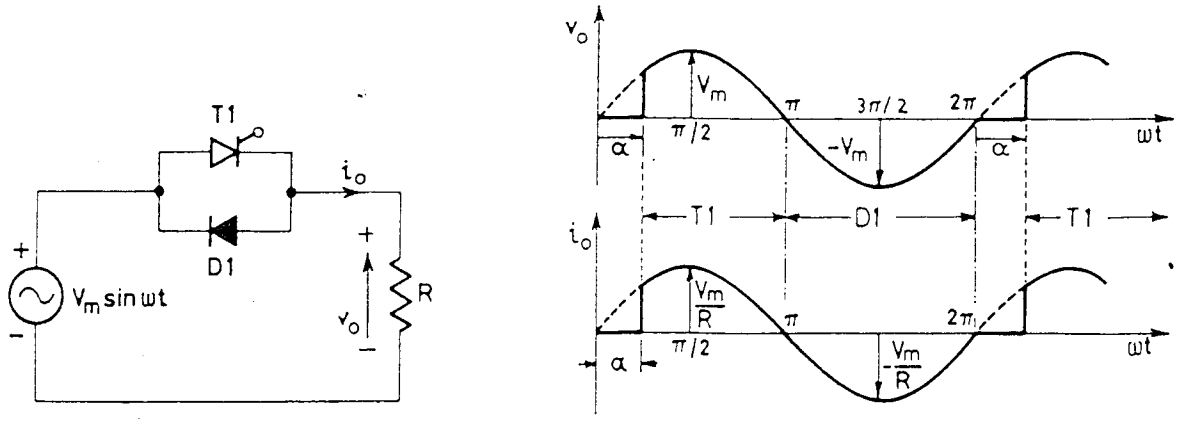
AC Voltage Controllers

AC voltage controllers are thyristor based devices which convert fixed alternating voltage directly to variable alternating voltage without a change in the frequency. Some of the main applications of ac voltage controllers are for domestic and industrial heating, transformer tap changing, lighting control, speed control of single-phase and three-phase ac drives and starting of induction motors. Earlier, the devices used for these applications were auto-transformers, tap-changing transformers, magnetic amplifiers, saturable reactors etc. But these devices are now replaced by thyristor-and triac-based ac voltage controllers because of their high efficiency, flexibility in control, compact size and less maintenance. AC voltage controllers are also adaptable for closed-loop control systems. Since the ac voltage controllers are phase-controlled devices, thyristors and triacs are line commutated and as such no complex commutation circuitry is required in these controllers. The main disadvantage of ac voltage controllers is the introduction of objectionable harmonics in the supply current and load voltage waveforms, particularly at reduced output voltage levels.

The object of this chapter is to study single-phase ac voltage controllers so far as their principle of working and gating signal requirements are concerned. Their use in transformer tap changers is also considered.

9.1. TYPES OF AC VOLTAGE CONTROLLERS

The power circuit diagram of a single-phase half-wave ac voltage controller using one thyristor in antiparallel with one diode is shown in Fig. 9.1 (*a*). In this figure, R is taken as



(*a*) (*b*)

Fig. 9.1. Single-phase half-wave ac voltage controller (*a*) Power-circuit diagram and (*b*) voltage and current waveforms.

the load for simplicity. The output voltage and current waveforms obtained from this controller are shown in Fig. 9.1 (*b*). It is seen from this figure that positive half cycle is not identical with negative half cycle for both voltage and current waveforms. As a result, dc component is introduced in the supply and load circuits which is undesirable.

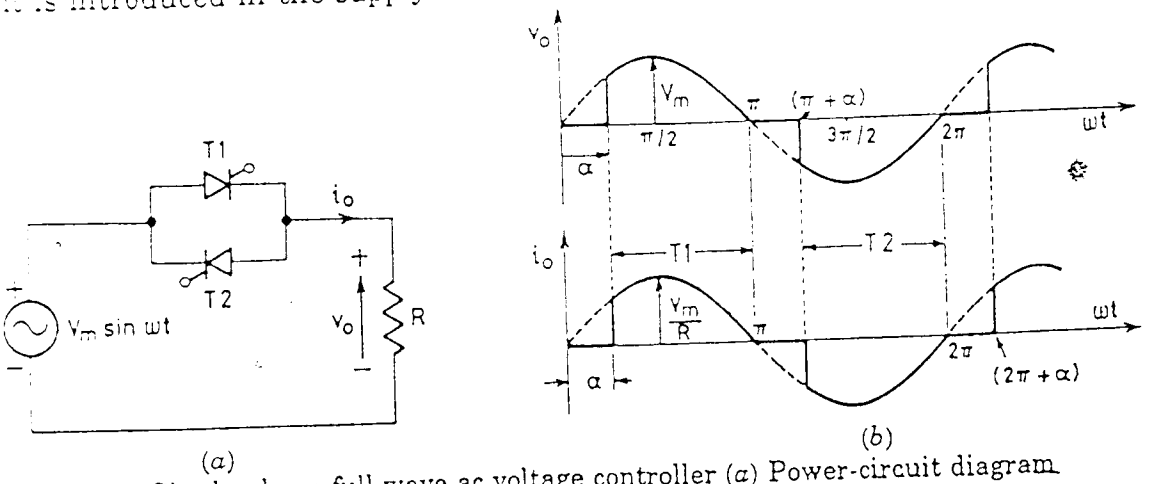


Fig. 9.2. Single-phase full-wave ac voltage controller (*a*) Power-circuit diagram and (*b*) voltage and current waveforms.

Fig. 9.2 (*a*) shows the power circuit diagram of a single-phase full-wave ac voltage controller with two SCRs connected in antiparallel. For this controller, voltage and current waveforms are shown in Fig. 9.2 (*b*). This figure reveals that positive half cycle is identical with negative half cycle for both voltage and current waveforms. The power circuit of Fig. 9.2 (*a*), therefore, introduces no direct component in the supply and load circuit. This circuit is thus more suited to practical circuits than single-phase half-wave circuit. In this chapter, therefore, only full-wave ac voltage controllers are described.

9.2. INTEGRAL CYCLE CONTROL

It is stated above that ac voltage controllers are phase-controlled devices. The principle of phase control is illustrated in Figs. 9.1 and 9.2. In these figures, the *phase* relationship between the start of load current and the supply voltage is *controlled* by varying the firing angle. As the controlled output is ac, these are called phase-controlled ac voltage controllers or ac voltage controllers.

In industry, there are several applications in which mechanical time constant or thermal time constant is of the order of several seconds. For example, mechanical time constant for many of the speed-control drives, or thermal time constant for most of the heating loads is usually quite high. For such applications, almost no variation in speed or temperature will be noticed if control is achieved by connecting the load to source for some on-cycles and then disconnecting the load for some off-cycles. This form of power control is called integral cycle control. So *integral cycle control* consists of switching on the supply to load for an integral number of cycles and then switching off the supply for a further number of integral cycles, Fig. 9.3

The principle of integral cycle control can be explained by referring to Fig. 9.2 for a single-phase voltage controller with resistive load. Gate pulses i_{g1}, i_{g2} turn on the thyristors T1, T2 respectively at zero-voltage crossing of the supply voltage. The source energises the load for n (= 3) cycles. When gate pulses are withdrawn, load remains off for m (= 2) cycles

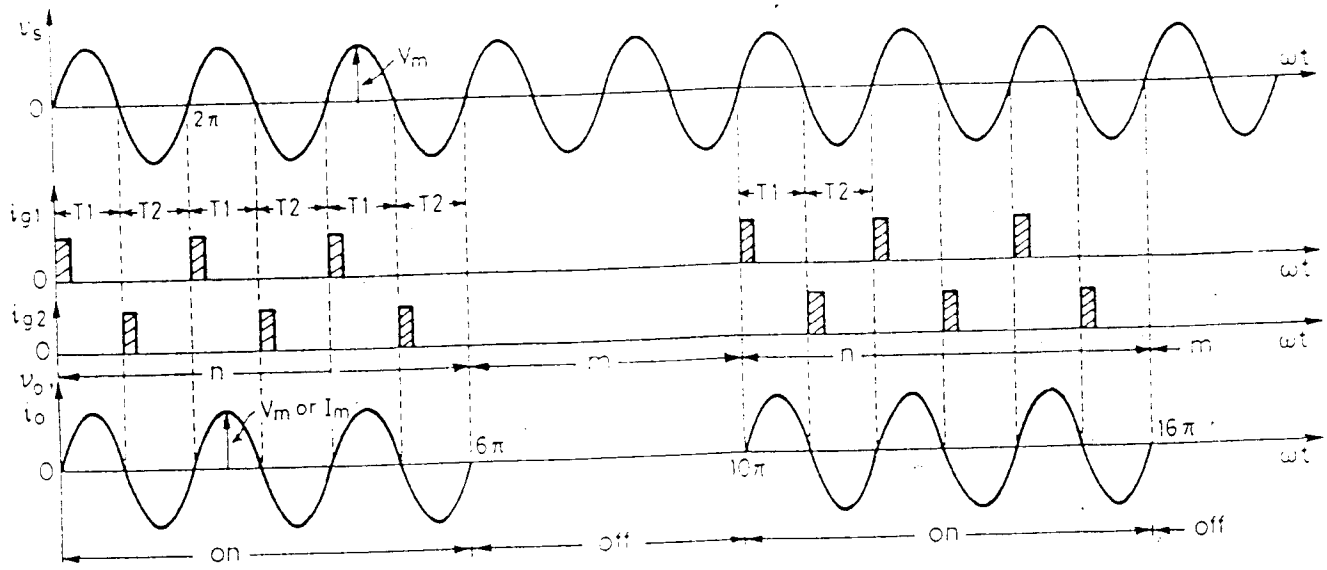


Fig. 9.3. Waveforms pertaining to integral cycle control.

for $n = 3$ and $m = 2$. Power is delivered to load for n cycles. No power is delivered to load for m cycles. It is the average power in the load that is controlled.

In literature, integral cycle control is also known as *on-off control, burst firing, zero-voltage switching, cycle selection* or *cycle syncopation.*

For sinusoidal supply voltage, the rms value of output voltage V_{or} can be obtained as under :

$$V_{or} = \frac{1}{\text{periodicity}}\left[\int_0^{2\pi} V_m^2 \sin^2 \omega t \, d(\omega t), \text{ for first on-cycle} + \int_0^{2\pi} V_m^2 \sin^2 \omega t \cdot d(\omega t), \text{ for second on-cycle} + \ldots\ldots + \int_0^{2\pi} V_m^2 \sin^2 \omega t \cdot d(\omega t), \text{ for } n\text{th on-cycle}\right]$$

For n on-cycles and m off-cycles, the periodicity $= (n + m)\, 2\pi$ radians, see Fig. 9.3.

$$\therefore \quad V_{or} = \left[\frac{n}{2\pi (n+m)} \int_0^{2\pi} V_m^2 \sin^2 \omega t \cdot d(\omega t)\right]^{1/2}$$

$$= \left[\frac{n V_m^2}{4\pi (n+m)} \int_0^{2\pi} (1 - \cos 2\omega t)\, d(\omega t)\right]^{1/2}$$

$$\text{or} \quad V_{or} = \frac{V_m}{\sqrt{2}} \cdot \sqrt{\frac{n}{n+m}} = V_s \sqrt{\frac{n}{n+m}} = V_s \sqrt{k} \qquad \ldots(9.1)$$

where V_s = rms value of source voltage

and $k = \dfrac{n}{n+m}$ is the duty cycle of ac voltage controller.

Rms load current, $I_{or} = \dfrac{V_{or}}{R}$

Power delivered to load $= \frac{V_{or}^2}{R} = \frac{V_s^2}{R}\left(\frac{n}{n+m}\right) = \frac{k \cdot V_s^2}{R}$ ...(9.2)

Rms value of input current, I_s = rms value of load current, I_{or}

Input $VA = V_s$ (rms value of source current)

$$= V_s \cdot I_s = V_s \cdot I_{or} = V_s \cdot \frac{V_{or}}{R}$$

Input VA × pf = power delivered to load

$\therefore$ Input pf $= \frac{V_{or}^2}{R} \cdot \frac{R}{V_s \cdot V_{or}} = \frac{V_{or}}{V_s} = \sqrt{\frac{n}{n+m}} = \sqrt{k}$ ...(9.3)

As each thyristor conducts for π radians during each cycle of n on-cycles, the average value of thyristor current is given by

$$I_{TA} = \frac{1}{2\pi}\int_0^{\pi} I_m \sin \omega t \cdot d(\omega t), \text{ for first on-cycle } +$$

$$\frac{1}{2\pi}\int_0^{\pi} I_m \cdot \sin \omega t \cdot d(\omega t), \text{ for second on-cycle } + \ldots\ldots +$$

$$\frac{1}{2\pi}\int_0^{\pi} I_m \cdot \sin \omega t \cdot d(\omega t), \text{ for } n\text{th on-cycle}]$$

$$= \frac{n}{2\pi(n+m)}\int_0^{\pi} I_m \cdot \sin \omega t \cdot d(\omega t)$$

$$= \frac{I_m}{\pi} \cdot \frac{n}{m+n} = \frac{k \cdot I_m}{\pi} \quad \ldots(9.4)$$

Similarly, rms value of thyristor current is

$$I_{TR} = \left[\frac{n}{2\pi(n+m)}\int_0^{\pi} I_m^2 \sin^2 \omega t \cdot d(\omega t)\right]^{1/2}$$

$$= \frac{I_m}{2}\sqrt{\frac{n}{n+m}} = \frac{I_m\sqrt{k}}{2} \quad \ldots(9.5)$$

Integral cycle control introduces less harmonics into the supply system, the supply undertakings therefore insist upon the consumers to use integral-cycle method for heating loads and for motor-control drives.

AC voltage controllers with on-off control has specific applications as discussed above. Phase-controlled ac voltage controllers are, however, more common. As such, phase-controlled ac voltage controllers will only be discussed and analysed in what follows :

Example 9.1. *A single-phase voltage controller has input voltage of 230 V, 50 Hz and a load of R = 15 Ω. For 6 cycles on and 4 cycles off, determine (a) rms output voltage, (b) input pf and (c) average and rms thyristor currents.*

Solution. (*a*) From Eq. (9.1), rms value of output voltage is

$$V_{or} = V_s\sqrt{\frac{n}{n+m}} = 230\sqrt{\frac{6}{6+4}} = 178.157 \text{ V}$$

(*b*) From Eq. (9.3), input pf $= \sqrt{k} = \sqrt{\frac{n}{n+m}} = \sqrt{\frac{6}{6+4}} = 0.7746$ lag.

Also power delivered to load $= I_{or}^2 R = \dfrac{V_{or}^2}{R} = \dfrac{178.157^2}{15} = 2116\ \text{W}$

Input VA $= 230 \times \dfrac{230\sqrt{6}}{15} = 2731.74\ \text{VA}$

$\therefore$ Input pf $= \dfrac{2116}{2731.74} = 0.7746\ \text{lag}$

(*c*) Peak thyristor current, $I_m = \dfrac{230\sqrt{2}}{15} = 21.681\ \text{A}$

From Eq. (9.4), average value of thyristor current,

$$I_{TA} = \frac{k I_m}{\pi} = \frac{0.6 \times 21.681}{\pi} = 4.1407\ \text{A}$$

From Eq. (9.5), rms value of thyristor current,

$$I_{TR} = \frac{I_m \cdot \sqrt{k}}{2} = \frac{21.681 \times \sqrt{0.6}}{2} = 8.397\ \text{A}$$

9.3. SINGLE-PHASE VOLTAGE CONTROLLERS

Fig. 9.4 shows three possible configurations of single-phase ac voltage controllers. Fig. 9.4 (*a*), similar to Fig. 9.2 (*a*), uses two thyristors connected in antiparallel. The trigger sources for the two thyristors must be isolated from one another because otherwise the two cathodes would be connected together and the two thyristors would be out of circuit as shown in Fig. 9.4 (*b*). Thus, no control of the output voltage would be possible.

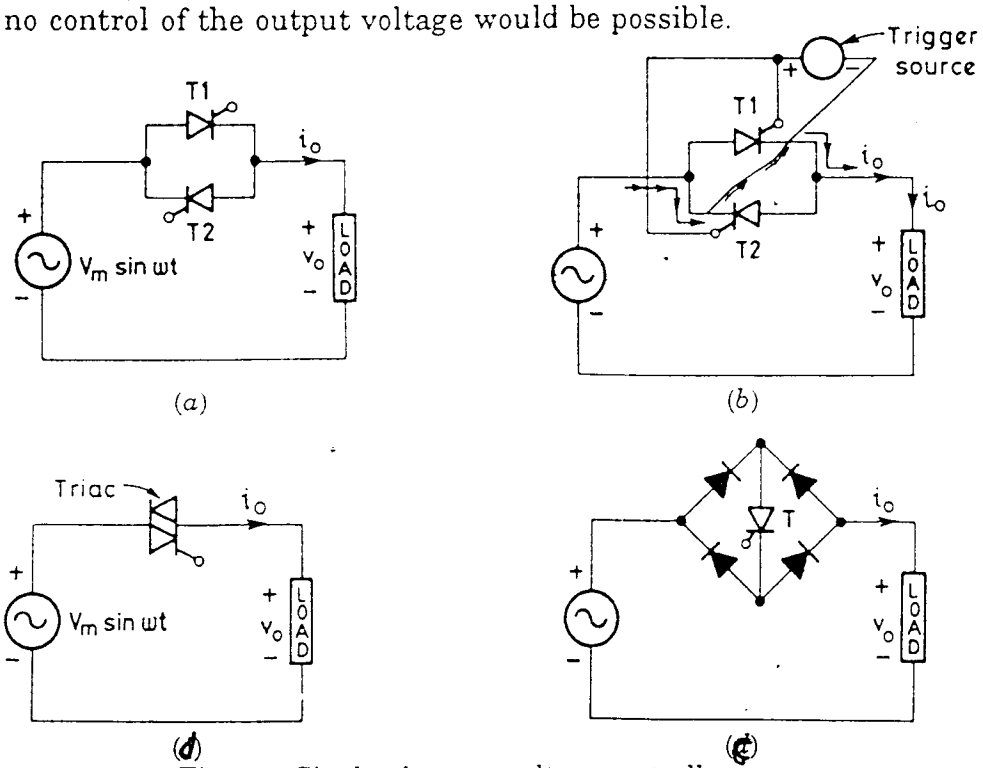


Fig. 9.4. Single-phase ac voltage controllers.

Scheme shown in Fig. 9.4 (*c*) employs four diodes and one thyristor. For this circuit, there is no need for any isolation between control and power circuits. This scheme, therefore offers a cheap ac voltage controller. The voltage drop in the three conducting devices (two diodes and one thyristor) will, however, be more than in Fig. 9.4 (*a*).

The circuit shown in Fig. 9.4 (*d*) uses one triac. This configurtion is suitable for low-power applications where the load is resistive or has only a small inductance. The triggering circuit for the triac need not be isolated from the power circuit.

9.3.1. Single-phase Voltage Controller with R Load

Fig. 9.5 (*a*) shows a single-phase voltage controller feeding power to a resistive load R. As stated before, two thyristors are connected in anti-parallel. Waveforms for source voltage v_s, gating pulses i_{g1}, i_{g2}, load current i_0, source current i_s, load voltage v_0, voltage across T1 as v_{T1} and that across T2 as v_{T2} are shown in Fig. 9.5 (*b*).

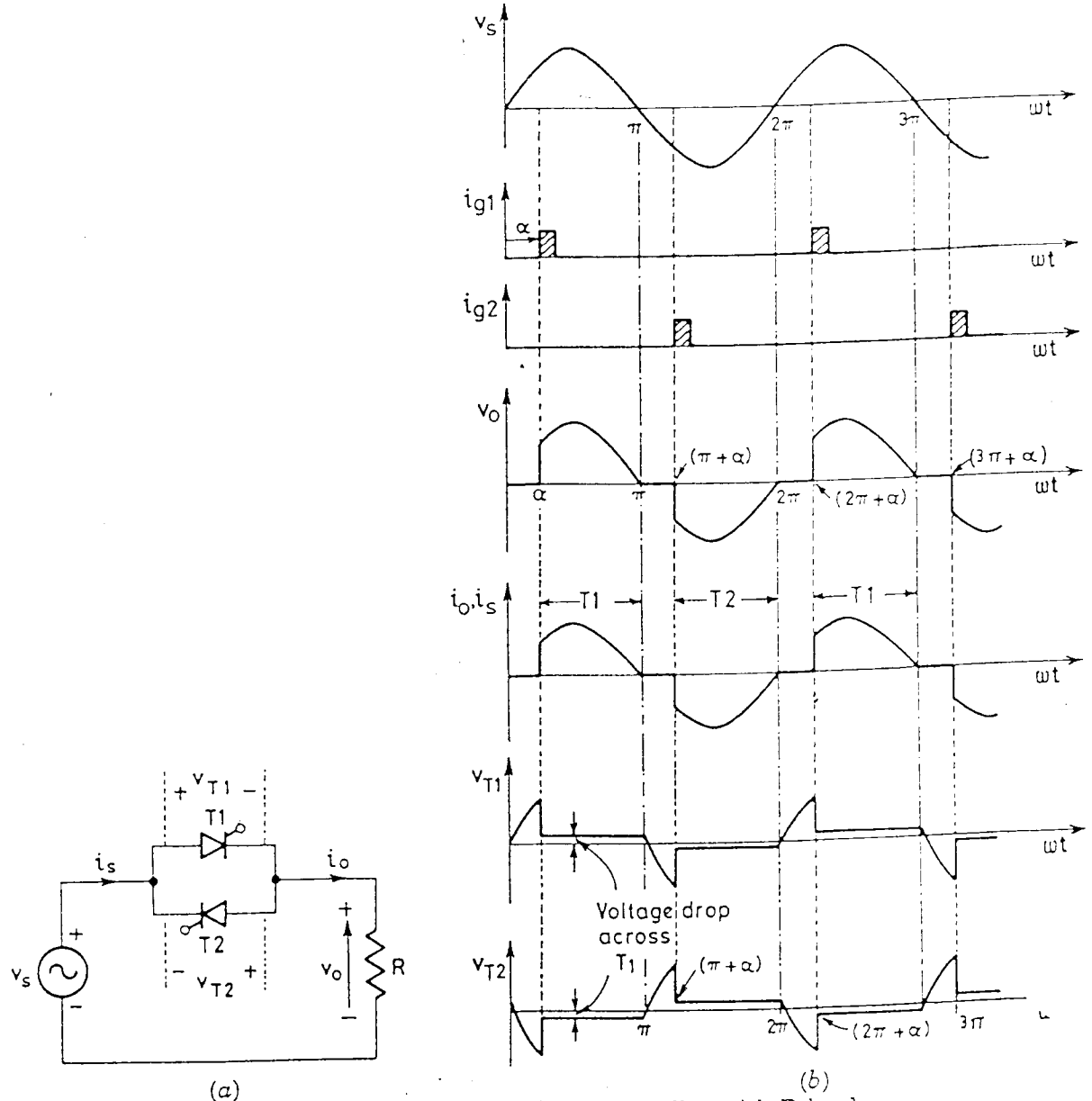


Fig. 9.5. (*a*) Single-phase ac voltage controller with R load
(*b*) Voltage and current waveforms for figure (*a*).

Thyristors T1 and T2 are forward biased during positive and negative half cycles respectively. During positive half cycle, T1 is triggered at a firing angle α. T1 starts conducting and source voltage is applied to load from α to π. At π, both v_0, i_0 fall to zero. Just after π, T1 is subjected to reverse bias, it is therefore turned off. During negative half cycle, T2 is triggered at (π + α). T2 conducts from π + α to 2π. Soon after 2π, T2 is subjected to a reverse bias, it is therefore commutated. Load and source currents have the same waveform.

From zero to α, T1 is forward biased, $v_{T1} = v_s$ as shown. From α, T1 conducts, v_{T1} is therefore about 1 V. After π, T1 is reverse biased by source voltage, therefore $v_{T1} = v_s$ from

π to $\pi + \alpha$. From $\pi + \alpha$ to 2π, T2 conducts ; T1 is therefore reverse biased by voltage drop across T2 which is about 1 to 1.5 V. The voltage variation v_{T1} across SCR T1 is shown in Fig. 9.5(*b*). Similarly, the variation of voltage v_{T2} across T2 can be drawn. In Fig. 9.5 (*b*), voltage drop across thyristors T1 and T2 is purposely shown just to highlight the duration of reverse bias across T1 and T2. Examination of this figure reveals that for any value of α, each thyristor is reverse biased for π/ω sec.

There is thus no restriction on the value of firing angle α. Firing angle can, therefore, be controlled from zero to π and rms output voltage from V_s to zero. Here V_s is the rms value of source voltage.

$\therefore$ Circuit turn-off time, $t_c = \dfrac{\pi}{\omega}$ sec.

Harmonics of output quantities and input current. It is seen from Fig. 9.5 (*b*) that waveforms for output quantities (voltage v_0 and current i_0) and input current i_s are non-sinusoidal. These waveforms can be described by Fourier series. As the positive and negative half cycles are identical, dc component and even harmonics are absent.

The output voltage v_0 can be represented by Fourier series as under :

$$v_0 = \sum_{n=1,3,5}^{\infty} A_n \sin n\omega t + \sum_{n=1,3,5}^{\infty} B_n \cos n\omega t \qquad ...(9.6)$$

where $$A_n = \frac{2}{\pi}\int_0^{\pi} v_0\,(\omega t)\sin n\omega t \cdot d(\omega t) \qquad ...(9.7)$$

and $$B_n = \frac{2}{\pi}\int_0^{\pi} v_0\,(\omega t)\cos n\omega t \cdot d(\omega t) \qquad ...(9.8)$$

The load voltage v_0 during the first half cycle is

$$v_0 = V_m \sin \omega t \ldots\ldots \alpha < \omega t < \pi \qquad ...(9.9)$$

Substitution of v_0 from Eq. (9.9) in Eqs. (9.7) and (9.8) gives

$$A_n = \frac{2V_m}{\pi}\int_{\alpha}^{\pi} \sin \omega t \cdot \sin n\omega t \cdot d(\omega t)$$

$$= \frac{V_m}{\pi}\int_{\alpha}^{\pi} [\cos (n-1)\,\omega t - \cos (n+1)\,\omega t]\, d(\omega t)$$

$$= \frac{V_m}{\pi}\left[\frac{\sin (n+1)\,\alpha}{n+1} - \frac{\sin (n-1)\,\alpha}{n-1}\right] \qquad ...(9.10)$$

and $$B_n = \frac{2V_m}{\pi}\int_{\alpha}^{\pi} \sin \omega t \cdot \cos n\omega t \cdot d(\omega t)$$

$$= \frac{V_m}{\pi}\int_{\alpha}^{\pi} [\sin (n+1)\,\omega t - \sin (n-1)\,\omega t]\, d(\omega t)$$

$$= \frac{V_m}{\pi}\left[\frac{\cos (n+1)\,\alpha - 1}{n+1} - \frac{\cos (n-1)\,\alpha - 1}{n-1}\right] \qquad ...(9.11)$$

where $V_m = \sqrt{2}\, V_s$ and V_s = rms value of source voltage .

For obtaining Eq. (9.11), note that for $n = 1, 3, 5 \ldots \cos (n+1)\,\pi = 1$ and $\cos (n-1)\,\pi = 1$.

The amplitude of the nth harmonic output voltage V_{nm} and its phase ϕ_n are given by

$$V_{nm} = \sqrt{A_n^2 + B_n^2} \text{ and } \phi_n = \tan^{-1} \frac{B_n}{A_n} \quad ...(9.12a)$$

and $$I_{nm} = \frac{V_{nm}}{R} = n\text{th harmonic load current} \quad ...(9.12b)$$

For fundamental frequency, *i.e.* for $n = 1$, V_{1m} and ϕ_1 cannot be obtained from Eqs. (9.10) to (9.12), because these become indeterminate for $n = 1$. This difficulty can, however, be overcome by putting $n = 1$ in Eqs. (9.7) and (9.8) and substituting the value of v_0 from Eq. (9.9).

$$\therefore \quad A_1 = \frac{2}{\pi}\int_{\alpha}^{\pi} V_m \sin^2 \omega t \cdot d(\omega t) = \frac{V_m}{\pi}\left[\frac{\sin 2\alpha}{2} + (\pi - \alpha)\right] \quad ...(9.13)$$

and $$B_1 = \frac{2}{\pi}\int_{\alpha}^{\pi} V_m \sin \omega t \cdot \cos \omega t \cdot d(\omega t) = \frac{V_m}{\pi}\left[\frac{\cos 2\alpha - 1}{2}\right] \quad ...(9.14)$$

From the coefficients A_1 and B_1, the peak value of the fundamental frequency voltage V_{1m} and its phase ϕ_1 are given by

$$V_{1m} = [A_1^2 + B_1^2]^{1/2}$$

$$= \frac{V_m}{\pi}\left[\left\{\frac{\sin 2\alpha}{2} + (\pi - \alpha)\right\}^2 + \left\{\frac{\cos 2\alpha - 1}{2}\right\}^2\right]^{1/2} \quad ...(9.15a)$$

$$I_{1m} = \frac{V_{1m}}{R} = \text{ amplitude of fundamental component of load or source current} \quad ...(9.15b)$$

and $$\phi_1 = \tan^{-1} \frac{B_1}{A_1} = \tan^{-1}\left[\frac{\cos 2\alpha - 1}{\sin 2\alpha + 2(\pi - \alpha)}\right] \quad ...(9.16)$$

When ac voltage controller is used for the speed control of a single-phase induction motor, only fundamental component is useful in producing the torque. The harmonics in the motor current merely increase the losses and therefore heating of the induction motor.

For heating and lighting loads, however, both fundamental and harmonics are useful in producing the ac controlled power. In such applications, rms value V_{or} of the output voltage should be known. It can be obtained from Eq. (9.9) as follows :

$$V_{or} = \left[\frac{1}{\pi}\int_{\alpha}^{\pi} V_m^2 \sin^2 \omega t \cdot d(\omega t)\right]^{1/2}$$

$$= \frac{V_m}{\sqrt{2}}\left[\frac{1}{\pi}\left\{(\pi - \alpha) + \frac{1}{2}\sin 2\alpha\right\}\right]^{1/2} \quad ...(9.17a)$$

and $$I_{or} = \frac{V_{or}}{R} = \text{ rms value of load, or source current} \quad ...(9.17b)$$

The average power P delivered to load of resistance R is

$$P = I_{or}^2 R = \frac{V_{or}^2}{R} = \frac{V_m^2}{2\pi R}\left[(\pi - \alpha) + \frac{1}{2}\sin 2\alpha\right]$$

$$= \frac{V_s^2}{\pi R}\left[(\pi - \alpha) + \frac{1}{2}\sin 2\alpha\right] \quad ...(9.18)$$

Maximum power P_{max} is delivered to load when $\alpha = 0$.

$$\therefore \qquad P_{max} = \frac{V_s^2}{\pi R}$$

This gives $$\frac{P}{P_{max}} = \left[(\pi - \alpha) + \frac{1}{2}\sin 2\alpha\right]$$

In terms of harmonic components,

$$P = R\,(I_{01}^2 + I_{03}^2 + I_{05}^2 + \ldots\ldots)$$

$$= \frac{1}{R}\,(V_{01}^2 + V_{03}^2 + V_{05}^2 + \ldots\ldots)$$

Fig. 9.5 (*b*) shows that source current waveform is identical with load current waveform. This shows that expressions for both load and source currents for the appropriate harmonics are the same.

Power Factor. Assuming that source voltage remains sinusoidal even though non-sinusoidal current is drawn from it, the power factor is given by

$$pf = \frac{\text{Real power}}{\text{Apparent power}} = \frac{V_s I_1 \cos\phi_1}{V_s \cdot I_{rms}} = \frac{I_1 \cdot \cos\phi_1}{I_{rms}} \qquad \ldots(9.19)$$

where $I_1 = \dfrac{I_{1m}}{\sqrt{2}}$ = rms value of fundamental component of source current given by Eq. (9.15 *b*)

$I_{rms} = I_{or}$ = rms value of source current, Eq. (9.17 *b*),

ϕ_1 = phase angle between V_s and I_1, Eq. (9.16)

Another expression for pf can be obtained as follows :

Real power delivered to load $= \dfrac{V_{or}^2}{R}$

Apparent power delivered to load

$$= V_s \cdot I_{or} = V_s \cdot \frac{V_{or}}{R}$$

$$\therefore \qquad pf = \frac{V_{or}^2/R}{V_s \cdot V_{or}/R} = \frac{V_{or}}{V_s}$$

From Eq. (9.17*a*), $$pf = \frac{V_{or}}{V_s} = \left[\frac{1}{\pi}\left\{(\pi - \alpha) + \frac{1}{2}\sin 2\alpha\right\}\right]^{1/2} \qquad \ldots(9.20)$$

The maximum value of rms output voltage and current occurs at $\alpha = 0$ and are given by V_s and V_s/R respectively, Eq. (9.17). For $\alpha = 0$, harmonics are absent, these are therefore also the maximum values of fundamental rms voltage and current.

Example 9.2. *A single-phase voltage controller feeds power to a resistive load of* 3 Ω *from 230 V, 50 Hz source. Calculate :*

(a) the maximum values of average and rms thyristor currents for any firing angle α,

(b) the minimum circuit turn-off time for any firing angle α,

(c) the ratio of third-harmonic voltage to fundamental voltage for $\alpha = \dfrac{\pi}{3}$,

(d) the maximum value of di/dt occurring in the thyristors,

(e) the angle α *at which the greatest forward or reverse voltage is applied to either of the thyristors and the magnitude of these voltages.*

considered here for describing the principle of operation of both the types of cycloconverters. A single-phase to single-phase device of the mid-point type is shown in Fig. 10.1 (*a*) and of the bridge type in Fig. 10.1 (*b*). With the help of this figure, the basic principles of both types of cycloconverters are described here.

10.1.1. Single-phase to Single-phase Circuit–Step-up Cycloconverter

For understanding the operating principle of step-up device, the load is assumed to be resistive for simplicity. It should be noted that a step-up cycloconverter requires forced commutation. The basic principle of step-up device is described here first for mid-point and then for bridge-type cycloconverters.

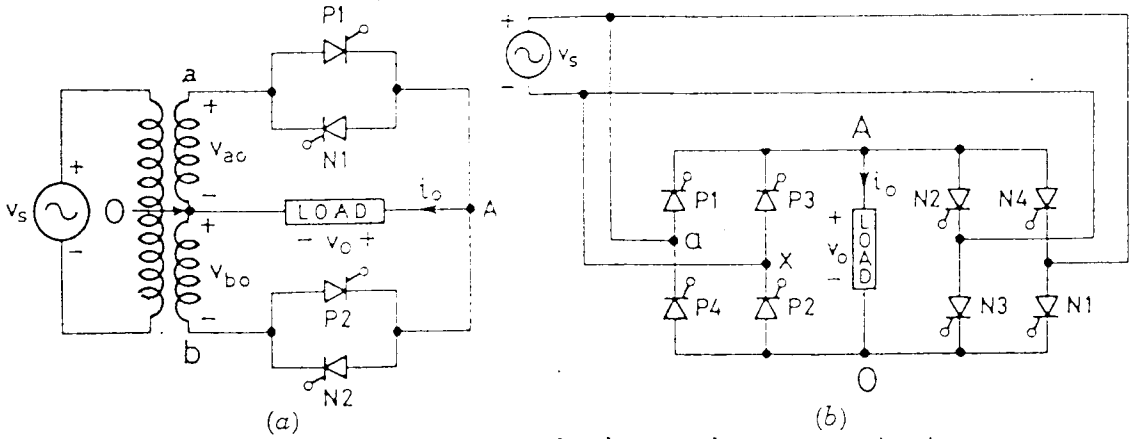


Fig. 10.1. Single-phase to single-phase cycloconverter circuit (*a*) mid-point type and (*b*) bridge type.

10.1.1.1. Mid-point cycloconverter. It consists of a single-phase transformer with mid-tap on the secondary winding and four thyristors. Two of these thyristors P1, P2 are for positive group and the other two N1, N2 are for the negative group. Load is connected between secondary winding mid-point 0 and terminal *A* as shown in Fig. 10.1 (*a*). Positive directions for output voltage v_0 and output current i_0 are marked in Fig. 10.1.

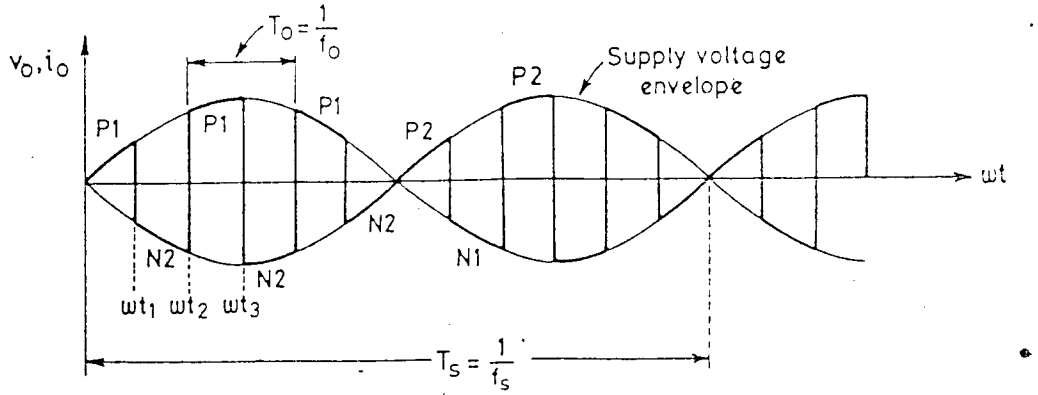


Fig. 10.2. Waveforms for step-up cycloconverter.

In Fig. 10.1, during the positive half cycle of supply voltage of Fig. 10.2, terminal *a* is positive with respect to terminal *b*. Therefore, in this positive half cycle, both SCRs P1 and N2 are forward biased from $\omega t = 0$ to $\omega t = \pi$. As such SCR P1 is turned on at $\omega t = 0°$ so that load voltage is positive with terminal *A* positive and 0 negative. The load voltage now follows the positive envelope of the supply voltage, Fig. 10.2. At instant ωt_1, P1 is force commutated and forward-biased thyristor N2 is turned on so that load voltage is negative with terminal 0 positive and *A* negative. The load, or output, voltage now traces the negative envelope of

TEN

Cycloconverters

A device which converts input power at one frequency to output power at a different frequency with one-stage conversion is called a cycloconverter. A cycloconverter is thus a one-stage frequency changer. Basically, cycloconverters are of two types, namely :

(*i*) step-down cycloconverters and

(*ii*) step-up cycloconverters.

In step-down cycloconverters, the output frequency f_0 is lower than the supply frequency f_s, *i.e.* $f_0 < f_s$. In step-up cycloconverters, $f_0 > f_s$.

The operating principles of step-down cycloconverters were developed as far back as 1930. At that time, mercury-arc rectifier was used as a cycloconverter for converting three-phase 50 Hz supply to single-phase $16\frac{2}{3}$ Hz supply for use in ac traction system in Germany. A single-phase series motor, when operated at a lower frequency, gives better operating characteristics. In the United States, a cycloconverter comprising 18 thyratrons was employed to drive a 400-HP synchronous motor for several years in Logan power station [6]. The cycloconverter systems at that time did not find widespread use only because early systems were not technically attractive and economically viable.

With the advent of high-power thyristors, cycloconverters are again becoming popular. At present, the applications of cycloconverters include the following :

(*i*) Speed control of high-power ac drives

(*ii*) Induction heating

(*iii*) Static VAR generation

(*iv*) For converting variable-speed alternator voltage to constant frequency output voltage for use as power supply in aircraft or shipboards.

The general use of cycloconverter is to provide either a variable frequency power from a fixed input frequency power (as in ac motor speed control) or a fixed frequency power from a variable input frequency power (as in aircraft or shipboard power supplies).

The object of this chapter is to present both single-phase and three-phase cycloconverters at an introductory level.

10.1. PRINCIPLE OF CYCLOCONVERTER OPERATION

In this section, basic principle of operation of step-up as well as step-down cycloconverter is presented. Single-phase to single-phase cycloconverter, though seldom used in practice, is

on. In this manner, a small delay in firing angle is introduced at C, D, E, F and G. At G, the firing angle is zero and the mean output voltage, given by $V_0 = V_{dc} \cos \alpha$, is maximum at G. At A, the mean output voltage is zero as $\alpha = 90°$. After point G, a small delay in firing angle is further introduced progressively at points H, I, J, K, L and M. At M, the firing angle is

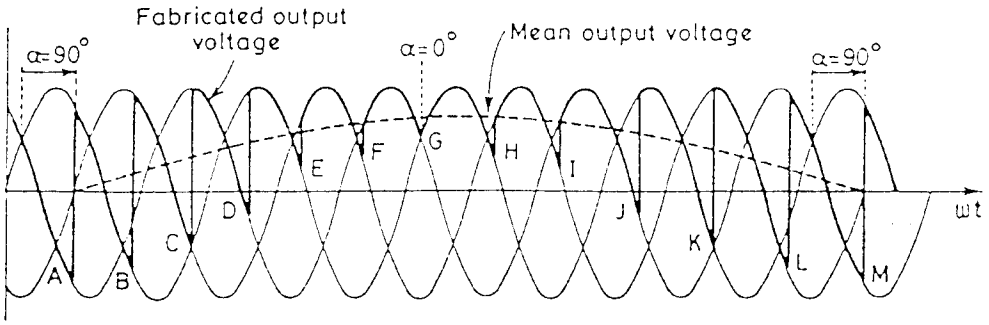


Fig. 10.5. Fabricated and mean output voltage waveforms for a single-phase cycloconverter.

again 90° and the value of mean output voltage is zero. The gating circuitry is suitably designed to introduce progressive firing angle delay as discussed here. In Fig. 10.5, the single-phase output voltage, fabricated from 3-phase input voltage, is shown by thick curve. Mean output voltage wave is obtained by joining points pertaining to average voltage values. For example, at A, $\alpha = 90°$, $V_0 = 0$; at G, $\alpha = 0°$, therefore V_0 has maximum mean output voltage and so on. It is seen from Fig. 10.5 that fabricated output voltage given by thick curve can be resolved into fundamental frequency output voltage plus several other harmonic components. The load inductance can, however, filter out the high-frequency unwanted harmonics. Fig. 10.5 reveals that for one half-cycle of fundamental frequency output voltage (marked mean output voltage in this figure), there are eight half cycles of supply frequency voltage. This shows that output frequency $f_0 = \frac{1}{8} f_s$ where f_s is the supply frequency.

It is obvious from Fig. 10.5 that for obtaining positive half cycle of low-frequency output voltage, firing angle is varied from 90° to zero degree and then to 90°. For obtaining one cycle (consisting of one positive half cycle and one negative half cycle) of low frequency output voltage, the firing angle should be varied from 90° to zero degree to 90° for positive half cycle and from 90° to 180° and back to 90° for negative half cycle. This is illustrated in Fig. 10.6.

It is thus seen from above that a complete cycle of low-frequency output voltage can be fabricated from the segments of 3-phase input voltage waveform by the use of phase-controlled converters. The cycloconverter can be made to deliver any pf load. In Fig. 10.6, the device is shown to deliver a lagging pf load. In a thyristor converter circuit, current can only flow in one direction. For allowing the flow of current in both the directions during one complete cycle of load current, two three-phase half-wave converters must be connected in antiparallel as shown in Fig. 10.7. The converter circuit that permits the flow of current during positive half cycle of low-frequency output current is called *positive converter group*. The other group permitting the flow of current during the negative half cycle of output current is called *negative converter group*. For a three-phase to single phase cycloconverter, schematic diagram is shown in Fig. 10.7 (*a*) and basic circuit configuration in Fig. 10.7 (*b*). This figure uses two 3-phase half wave converters in anti-parallel, the positive group for the conduction of positive load current and the negative group for the flow of negative load current.

Examination of Fig. 10.6 reveals that when output current is positive (above the reference line) positive converter conducts. Under this condition, positive converter acts as a rectifier when output voltage is positive and as an inverter when output voltage is negative. When

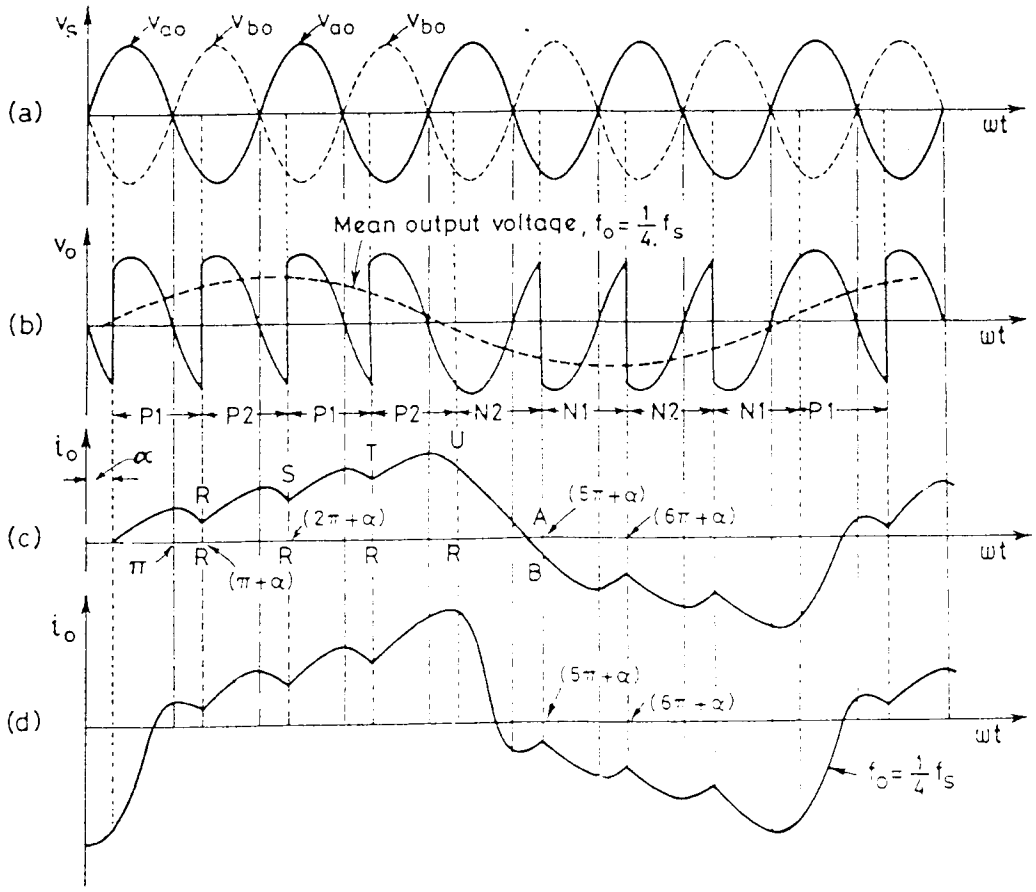


Fig. 10.4. Voltage and current waveforms for step-down cycloconverter with continuous load current.

waveform is redrawn in Fig. 10.4 (*d*) under steady state conditions. It is seen from load current waveform that i_0 is symmetrical about ωt axis in Fig. 10.4 (*d*). The positive group of voltage group and current wave consists of four pulses and same is true for negative group of wave. One positive group of pulses along with one negative group of identical pulses constitute one cycle for the load voltage and load current. The supply voltage has, however, gone through four cycles. The output frequency is, therefore, $f_0 = \frac{1}{4} f_s$ in Fig. 10.4.

10.1.2.2. Bridge-type cycloconverter. The operation of bridge type cycloconverter shown in Fig. 10.1 (*b*) can be easily explained for both discontinuous and continuous load currents. The voltage and current waveforms would again be as shown in Fig. 10.3 for discontinuous load current and as in Fig. 10.4 for continuous load current. The explanation of bridge-type cycloconverter is left as an exercise to the reader.

10.2. THREE-PHASE HALF-WAVE CYCLOCONVERTER

The object of this section is to consider how single-phase low-frequency output voltage is fabricated from the segments of 3-phase input voltage waveform. Then three-phase to three-phase cycloconverters are described.

10.2.1. Three-phase to Single-phase Cycloconverters

For converting three-phase supply at one frequency to single-phase supply at a lower frequency, the basic principle is to vary progressively the firing angle of the three thyristors of a 3-phase half-wave circuit. In Fig. 10.5, firing angle at *A* to 90°, at *B* firing angle is somewhat less than 90°, at *C* the firing angle is still further reduced than it is at *B* and so

$\omega t = \pi$, terminal b is positive with respect to terminal a ; both SCRs P2 and N1 are therefore forward biased from $\omega t = \pi$ to 2π. At $\omega t = \pi$, N2 is force commutated and forward biased SCR P2 is turned on. At $\omega t = \frac{1}{2_{fs}} + \frac{1}{2_{fo}}$, P2 is force commutated and forward biased SCR N1 is turned on. In this manner, thyristors P1, N2 for first half cycle ; P2, N1 in the second half cycle and so on are switched alternately between positive and negative envelopes at a high frequency. As a result, output voltage of frequency f_0, higher than the supply frequency f_s, is obtained. In Fig. 10.2, f_s is the supply frequency and f_0 is the output frequency. Also $f_0 = 6 f_s$ in Fig. 10.2.

10.1.1.2. Bridge-type cycloconverter. It consists of a total of eight thyristors, P1 to P4 *i.e.* four for positive group and the remaining four for the negative group. When a is positive with respect to x in Fig. 10.1 (*b*), *i.e.* during the positive half cycle of supply voltage of Fig. 10.2, thyristor pairs P1, P2 and N1, N2 are forward biased from $\omega t = 0°$ to $\omega t = \pi$. When forward biased thyristors P1, P2 are turned on together at $\omega t = 0°$, the load voltage is positive with respect to x in Fig. 10.1 (*b*), forward-biased thyristors P1, P2 are turned on together at $\omega t = 0°$ so that load voltage is positive with terminal A positive with respect to 0. Load voltage now traverses the positive envelope of supply voltage, Fig. 10.2. At ωt_1, pair P1, P2 is force commutated and forward biased pair N1, N2 is turned on. With this, load voltage is negative with terminal 0 positive with respect to A. Load voltage now follows the negative envelope of source voltage, Fig. 10.2. At ωt_2 ; N1, N2 are force commutated and P1, P2 are turned on. The load voltage is now positive and follows the positive envelope of source voltage. After $\omega t = \pi$, thyristor pairs P3, P4 and N3, N4 are forward biased, these can therefore be turned on and force commutated from $\omega t = \pi$ to $\omega t = 2\pi$. In this manner, a high-frequency turning-on and force commutation of pairs P1, P2, N1 N2 and pairs P3 P4, N3 N4 gives a carrier-frequency modulated output voltage across load terminals.

In Fig. 10.2 conduction of thyristors P1, P2 and N1, N2 for mid-point cycloconverter of Fig. 10.1 (*a*) is only shown. It is fairly easy to indicate the conduction of thyristors P1 to P4 and N1 to N4 in Fig. 10.2.

10.1.2. Single-phase to Single-phase Circuit–Step-down Cycloconverter

A step-down cycloconverter does not require forced commutation. It requires phase-controlled converters connected as shown in Fig. 10.1. These converters need only line, or natural, commutation which is provided by ac supply. Both mid-point and bridge-type cycloconverters are described in what follows :

10.1.2.1. Mid-point cycloconverter. This type of cycloconverter will be described both for discontinuous as well as continuous load current. The load is now assumed to consist of R and L in series.

(*a*) **Discontinuous load current.** When a is positive with respect to 0 in Fig. 10.1 (*a*), forward biased SCR P1 is triggered at $\omega t = \alpha$. With this, load current i_0 starts building up in the positive direction from A to O. Load current i_0 becomes zero at $\omega t = \beta > \pi$ but less than $(\pi + \alpha)$, Fig. 10.3 (*c*). Thyristor P1 is thus naturally commutated at $\omega t = \beta$ which is already reverse biased after π. After half a cycle, b is positive with respect to 0. Now forward biased thyristor P2 is triggered at $\omega t = \pi + \alpha$. Load current is again positive from A to O and builds up from zero as shown in Fig. 10.3 (*c*). At $\omega t = \pi + \beta$, i_0 decays to zero and P2 is naturally commutated. At $2\pi + \alpha$, P1 is again turned on. Load current in Fig. 10.3 (*c*) is seen to be discontinuous. After four positive half cycles of load voltage and load current, thyristor N2 after P2. N2 should be fired) is gated at $(4\pi + \alpha)$ when 0 is positive with respect to b. As N2

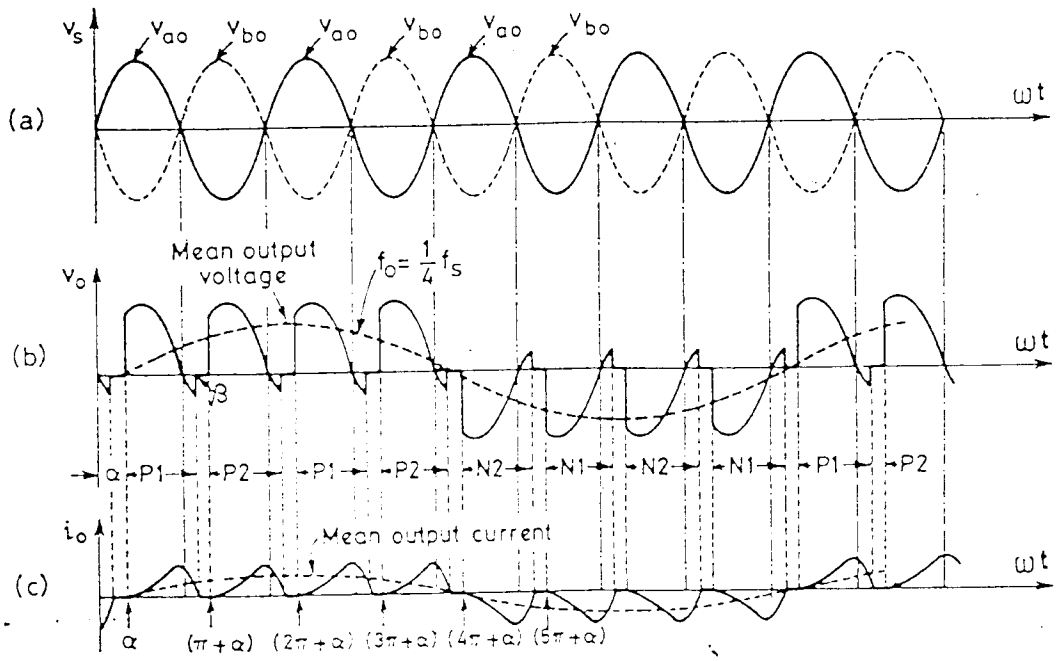


Fig. 10.3. Voltage and current waveforms for step-down cycloconverter with discontinuous load current.

is forward biased, it starts conducting but load current direction is reversed, *i.e.* it is now from 0 to *A*. After N2 is triggered, load current builds up in the negative direction as shown in Fig. 10.3 (*c*). In the next half-cycle, 0 is positive with respect to *a* but before N1 is fired, i_0 decays to zero and N2 is naturally commutated. Now when N1 is gated at $(5\pi + \alpha)$, i_0 again builds up but it decays to zero before thyristor N2 in sequence is again gated. In this manner, four negative half cycles of load voltage and load current, equal to the number of four positive half cycles, are generated. Now P1 is again triggered to fabricate further four positive half cycles of load voltage and so on. For discontinuous load current, natural commutation is achieved, *i.e.* P1 goes to blocking state before P2 is gated and so on.

In Fig. 10.3, mean output voltage and current waves are also shown. It is seen from this figure that frequency of output voltage and current is $f_0 = \frac{1}{4} f_s$.

(*b*) **Continuous load current.** When *a* is positive with respect to 0 in Fig. 10.1 (*a*), P1 is triggered at $\omega t = \alpha$, positive output voltage appears across load and load current starts building up, Fig. 10.4 (*c*). At $\omega t = \pi$, supply and load voltages are zero. After $\omega t = \pi$, P1 is reverse biased. As load current is continuous, P1 is not turned off at $\omega t = \pi$. When P2 is triggered in sequence at $\pi + \alpha$, a reverse voltage appears across P1, it is therefore turned off by natural commutation. When P1 is commutated load current has built up to a value equal to *RR*, Fig. 10.4 (*c*). With the turning on of P2 at $(\pi + \alpha)$, output voltage is again positive as it was with P1 on. As a consequence, load current builds up further than *RR* as shown in Fig. 10.4 (*c*). At $(2\pi + \alpha)$, when P1 is again turned on, P2 is naturally commutated and load current through P1 builds up beyond *RS* as shown. At the end of four positive half cycles of output voltage, load current is *RU*. When N2 is now triggered after P2, load is subjected to a negative voltage cycle and load current i_0 decreases from positive *RU* to negative *AB* (say) as shown in Fig. 10.4 (*c*). Now N2 is commutated and N1 is gated at $(5\pi + \alpha)$. Load current i_0 becomes more negative than *AB* at $(6\pi + \alpha)$, this is because with N1 on, load voltage is negative. For four negative half cycles of output voltage, current i_0 is shown in Fig. 10.4 (*c*). Load current