2 Logic Gates

A logic gate is an electronic circuit which makes logic decisions. It has one output and one or more inputs.

THE INVERTER

The inverter (NOT circuit) performs the operation called inversion or complementation. The inverter changes one logic level to the opposite level. In terms of bits, it changes a 1 to a 0 and a 0 to a 1.

Standard logic symbols for the inverter are shown in Fig.(2-1), shows the distinctive shape symbols.
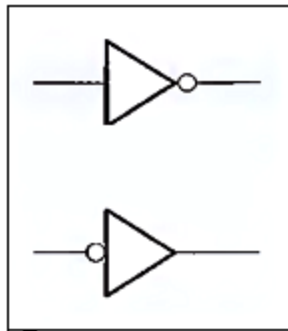

Fig.(2-1) Logic symbol for the inverter.

When a HIGH level is applied to an inverter input, a LOW level will appear on its output. When a LOW level is applied to its input, a HIGH will appear on its output as shown in Fig.(2-2). This operation is summarized in Table 2-1, which shows the output for each possible input in terms of levels and corresponding bits. A table such as this is called a ***truth table***, which gives the output state for all possible input combinations.

Table 2-1

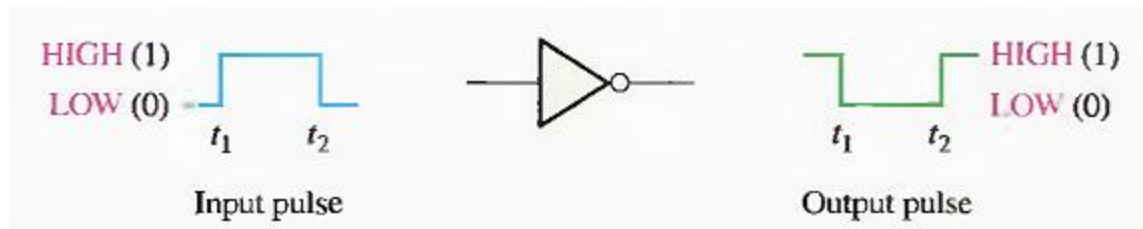| INPUT	OUTPUT
LOW (0)	HIGH (1)
HIGH (1)	LOW (0)

Fig.(2-2) Inverter operation.

The operation of an inverter (NOT circuit) can be expressed as follows: If the input variable is called A and the output variable is called X, then

$$X = \overline{A}$$

This expression states that the output is the complement of the input, so if A = 0, then X = 1, and if A = 1, then X = 0.

The AND Gate

The term gate is used to describe a circuit that performs a basic logic operation. The AND gate is composed of two or more inputs and a single output, as indicated by the standard logic symbols shown in Fig.(2-3). Inputs are on the left, and the output is on the right in each symbol. Gates with two inputs are shown; however, an AND gate can have any number of inputs greater than one.
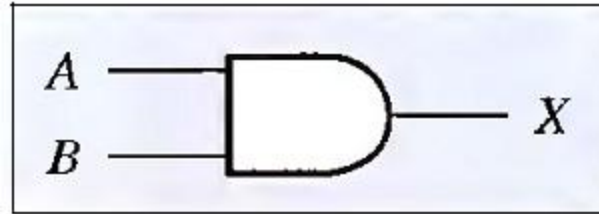
Fig.(2-3) AND gate symbol.

Operation of an AND Gate

An AND gate produces a HIGH output only when all of the inputs are HIGH. When any of the inputs is LOW, the output is LOW. Therefore, the basic purpose of an AND gate is to determine when certain conditions are simultaneously true, as indicated by HIGH levels on all of its inputs, and to produce a HIGH on its output to indicate that all these conditions are true. The inputs of the 2-input AND gate in Fig.(2-3) are labelled A and B, and the output is labelled X. The gate operation can be stated as follows:

For a 2-input AND gate, output X is HIGH only when inputs A and B are HIGH; X is LOW when either A or B is LOW, or when both A and B are LOW.
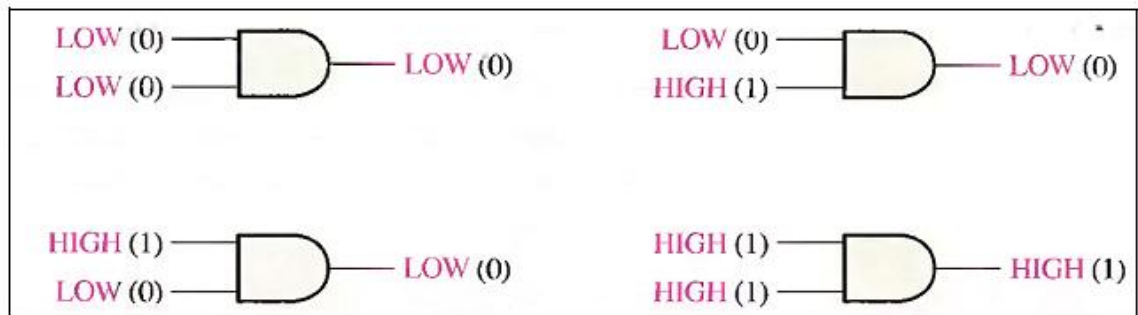

Fig.(2-4) All possible logic levels for a 2-input AND gate.

The logical operation of a gate can be expressed with a truth table that lists all input combinations with the corresponding outputs, as illustrated in Table 2-2 for a 2-input AND gate. The truth table can be expanded to any number of inputs. For any AND gate, regardless of the number of inputs, the output is HIGH only when all inputs are HIGH.

Table 2-2 The truth table for a 2-input AND gate.

INPUTS		OUTPUT
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

1 = HIGH, 0 = LOW

The total number of possible combinations of binary inputs to a gate is determined by the following formula:

$$N = 2^n$$

where N is the number of possible input combinations and n is the number of input variables. To illustrate:

For two input variables: $N = 2^2 = 4$ combinations.

For three input variables: $N = 2^3 = 8$ combinations.

For four input variables: $N = 2^4 = 16$ combinations.

Q/ Develop the truth table for a 3-input AND gate.

Let's examine the waveform operation of an AND gate by looking at the inputs with respect to each other in order to determine the output level at any given time. In Fig.(2-5), inputs A and B are both HIGH (1) during the time interval, t_1 making output X HIGH (1) during this interval. During time interval t_2 input A is LOW (0) and input B is HIGH (1), so the output is LOW (0). During time interval t_3 , both inputs are HIGH (1), and therefore the output is HIGH (1). During time interval t_4 , input A is HIGH 0) and input B is LOW (0), resulting in a LOW (0) output. Finally, during time interval t_5 , input A is LOW (0), input B is LOW (0), and the output is therefore LOW (0). As you know, a diagram of input and output waveforms showing time relationships is called a timing diagram.
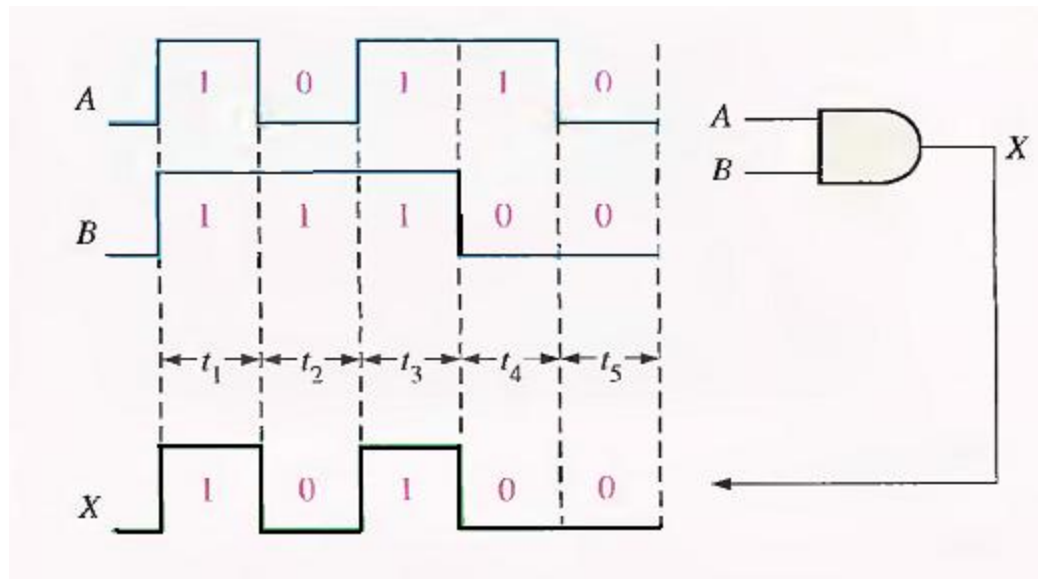

Fig.(2-5) Example of AND gate operation with a timing diagram showing input and output relationships.

Logic Expressions for an AND Gate

The logical AND function of two variables is represented mathematically either by placing a dot between the two variables, as A . B, or by simply writing the adjacent letters without the dot, as AB. We will normally use the latter notation because it is easier to write.

Boolean multiplication follows the same basic rules governing binary multiplication:

$$0 . 0 = 0$$
$$0 . 1 = 0$$
$$1 . 0 = 0$$
$$1 . 1 = 1$$

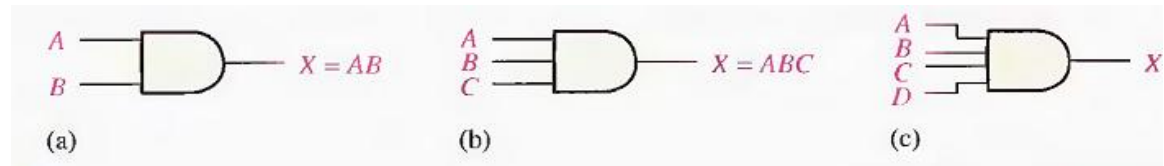**Boolean multiplication is the same as the AND function.**

Fig.(2-6) Boolean expressions for AND gates with two, three, and four inputs.

The OR Gate

An OR gate can have more than two inputs. The OR gate is another of the basic gates from which all logic functions are constructed. An OR gate can have two or more inputs and performs what is known as logical addition.

An OR gate has two or more inputs and one output, as indicated by the standard logic symbol in Fig.(2-7), where OR gates with two inputs are illustrated. An OR gate can have any number of inputs greater than one.
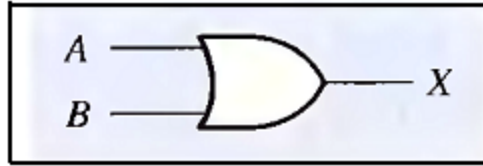
Fig.(2-7) Standard logic symbol for the OR gate.

Operation of an OR Gate

An OR gate produces a HIGH on the output when any of the inputs is HIGH. The output is LOW only when all of the inputs are LOW.

The inputs of the 2-input OR gate in Fig.(2-7) are labelled A and B. and the output is labelled X. The operation of the gate can be stated as follows:

For a 2-input OR gate, output X is HIGH when either input A or input B is HIGH, or when both A and B are HIGH; X is LOW only when both A and B are LOW.

The HIGH level is the active or asserted output level for the OR gate. Fig.(2-8) illustrates the operation for a 2-input OR gate for all four possible input combinations.

Fig.(2-8) All possible logic levels for a 2-input OR gate.

OR Gate Truth Table

The operation of a 2-input OR gate is described in Table 2-3. This truth table can be expanded for any number of inputs; but regardless of the number of inputs. the output is HIGH when one or more of the inputs are HIGH.

Table 2-3 The truth table for a 2-input OR gate.

INPUTS		OUTPUT
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

1 = HIGH, 0 = LOW

Operation with Waveform Inputs

Now let's look at the operation of an OR gate with pulse waveform inputs, keeping in mind its logical operation. Again, the important thing in the analysis of gate operation with pulse waveforms is the time relationship of all the waveforms involved. For example, in Fig.(2-9), inputs A and B are both HIGH (1) during time interval t_1 making output X HIGH (1). During time interval t_2, input A is LOW (0), but because input B is HIGH (1), the output is HIGH (1). Both inputs are LOW (0) during time interval t_3 , so there is a LOW (0) output during this time. During time interval t_4 , the output is HIGH (1) because input A is HIGH (1).
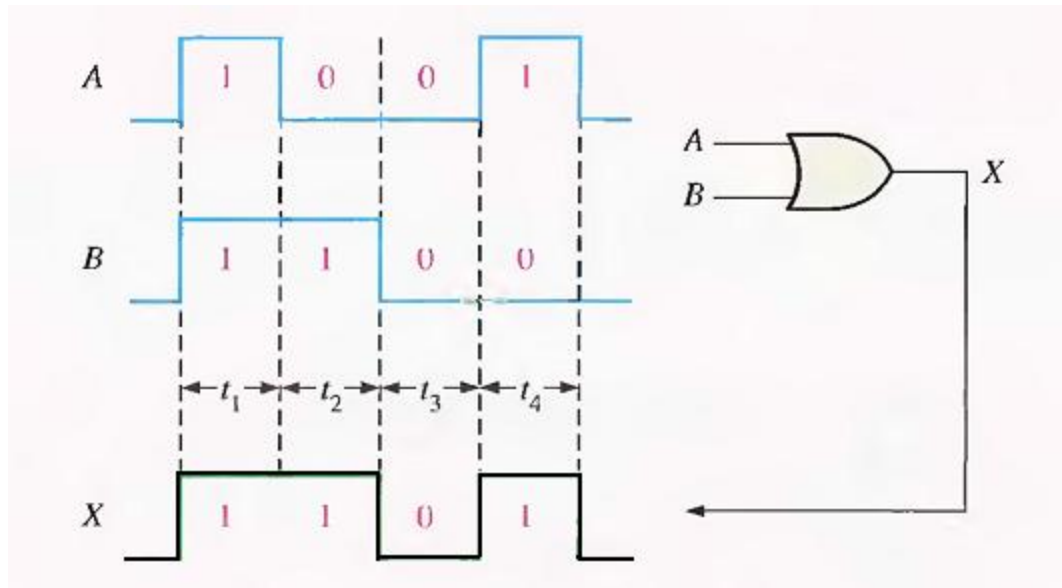
Fig.(2-9)) Example of OR gate operation with a timing diagram showing input and output relationships.

Logic Expressions for an OR Gate

The logical OR function of two variables is represented mathematically by a + between the two variables, for example, A + B.

Addition in Boolean algebra involves variables whose values are either binary 1 or binary 0. The basic rules for Boolean addition are as follows:

$$0 + 0 = 0$$
$$0 + 1 = 1$$
$$1 + 0 = 1$$
$$1 + 1 = 1$$

Boolean addition is the same as the OR function.

Notice that Boolean addition differs from binary addition in the case where two 1 s are added. There is no carry in Boolean addition.

The operation of a 2-input OR gate can be expressed as follows: If one input variable is A, if the other input variable is B, and if the output variable is X, then the Boolean expression is

$$X=A+B$$

Fig.(2-10)(a) shows the OR gate logic symbol with two input variables and the output variable labelled.
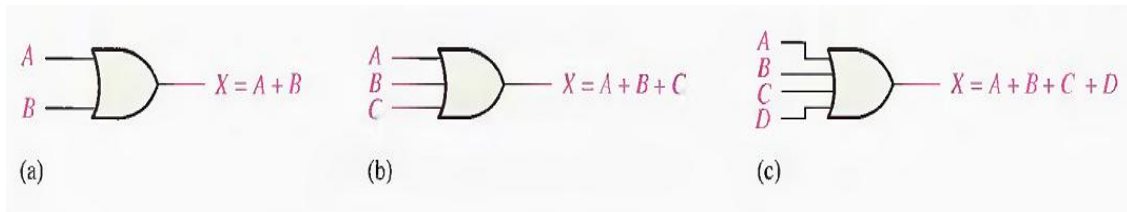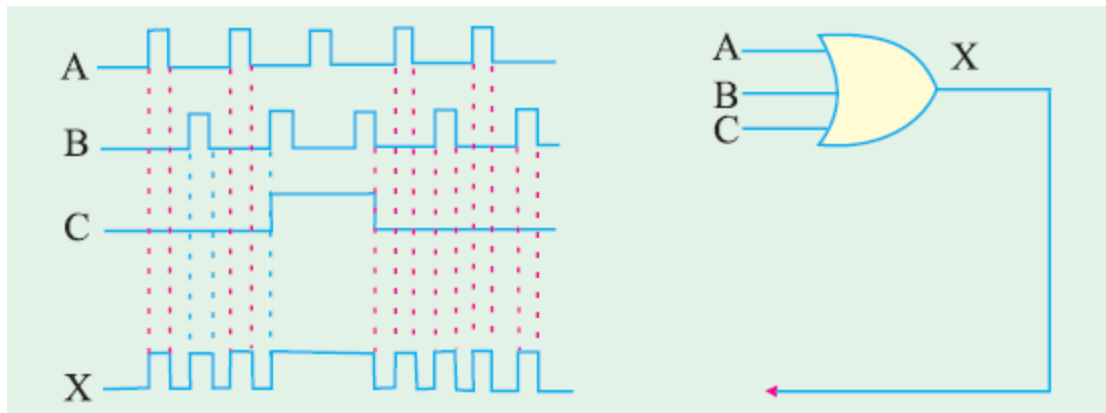

Fig.(2-10) Boolean expressions for OR gates with two, three, and four inputs.

To extend the OR expression to more than two input variables. a new letter is used for each additional variable. For instance, the function of a 3-input OR gate can be expressed as $X = A + B + C$. The expression for a 4-input OR gate can be written as $X = A + B + C + D$, and so on. Parts (b) and (c) of Fig.(2-10) how OR gates with three and four input variables, respectively.

Ex: For a three-input OR gate shown in Figure below, determine the output waveform.

THE NAND GATE

The NAND gate is a popular logic element because it can be used as a universal gate: that is, NAND gates can be used in combination to perform the AND, OR, and inverter operations.

The term NAND is a contraction of NOT-AND and implies an AND function with a complemented (inverted) output. The standard logic symbol for a 2-input NAND gate and its equivalency to an AND gate followed by an inverter are shown in Fig.(2-11)(a), where the symbol ≡ means equivalent to. A rectangular outline symbol is shown in part (b).
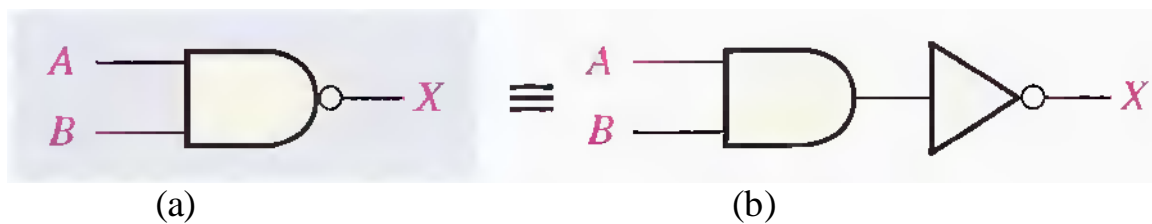

(a)   (b)

Fig.(2-11) Standard NAND gate logic symbols.
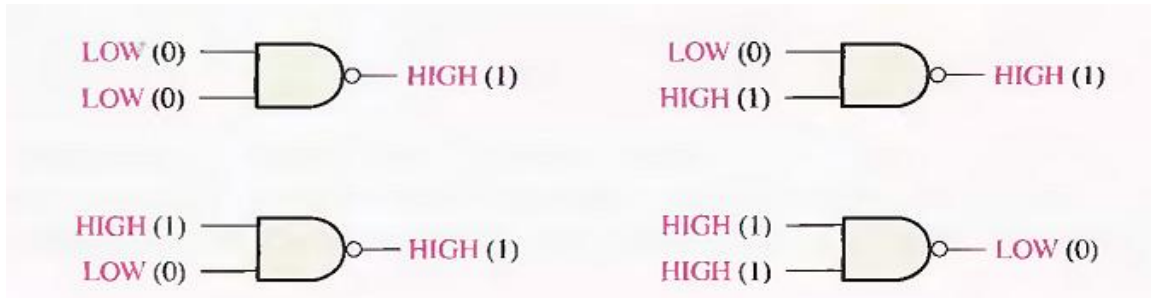
Operation of a NAND Gate

A NAND gate produces a LOW output only when all the inputs are HIGH. When any of the inputs is LOW, the output will be HIGH. For the specific case of a 2-input NAND gate, as shown in Fig.(2-11) with the inputs labelled A and B and the output labelled X, the operation can be stated as follows:

For a 2-input NAND gate, output X is LOW only when inputs A and B are HIGH; X is HIGH when either A or B is LOW, or when both A and B are LOW.

Note that this operation is opposite that of the AND in terms of the output level. In a NAND gate, the LOW level (0) is the active or asserted output level, as indicated by the bubble on the output. Fig.(2-12) illustrates the operation of a 2-input NAND

gate for all four input combinations, and Table 2-4 is the truth table summarizing the logical operation of the 2-input NAND gate.

The NAND is the same as the AND except the output is inverted.

Fig.(2-12) Operation of a 2-input NAND gate.

Table 2-4 Truth table for a 2-input NAND gate.

INPUTS		OUTPUT
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

1 = HIGH, 0 = LOW.

Negative-OR Equivalent Operation of a NAND Gate

Inherent in a NAND gate's operation is the fact that one or more LOW inputs produce a HIGH output. Table 2-4 shows that output X is HIGH (1) when any of the inputs, A and B, is LOW (0). From this viewpoint, a NAND gate can be used for an OR operation that requires one or more LOW inputs to produce a HIGH output. This aspect of NAND operation is referred to as negative-OR. The term

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negative in this context mean that the inputs are defined to be in the active or asserted state when LOW.

For a 2-input NAND gate performing a negative-OR operation, output X is HIGH when either input A or input B is LOW, or when both A and B are LOW.

When a NAND gate is used to detect one or more LOWs on its inputs rather than all HIGHs, it is performing the negative-OR operation and is represented by the standard logic symbol shown in Fig.(2-13).
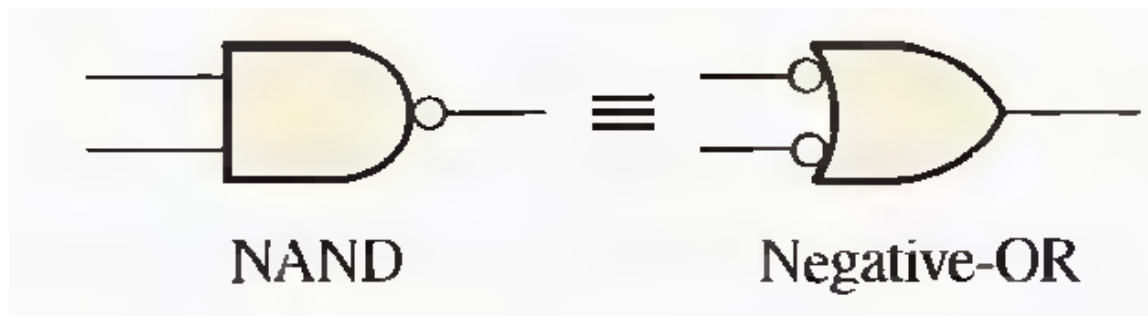

Fig.(2-13) Standard symbols representing the two equivalent operation of a NAND gate.

Logic Expressions for a NAND Gate

The Boolean expression for the output of a 2-input NAND gate is

$$X = \overline{AB}$$

This expression says that the two input variables, A and B, are first ANDed and then complemented, as indicated by the bar over the AND expression. This is a description in equation form of the operation of a NAND gate with two inputs. Evaluating this expression for all possible values of the two input variables, you get the results shown in Table 2-5.

Table 2-5.

A	B	$\overline{AB} = X$
0	0	$\overline{0 \cdot 0} = \overline{0} = 1$
0	1	$\overline{0 \cdot 1} = \overline{0} = 1$
1	0	$\overline{1 \cdot 0} = \overline{0} = 1$
1	1	$\overline{1 \cdot 1} = \overline{1} = 0$

The NOR Gate

The NOR gate, like the NAND gate, is a useful logic element because it can also be used as a universal gate; that is, NOR gates can be used in combination to perform the AND, OR, and inverter operations.

The term NOR is a contraction of NOT-OR and implies an OR function with an inverted (complemented) output. The standard logic symbol for a 2-input NOR gate and its equivalent OR gate followed by an inverter are shown in Fig.(2-14)(a).
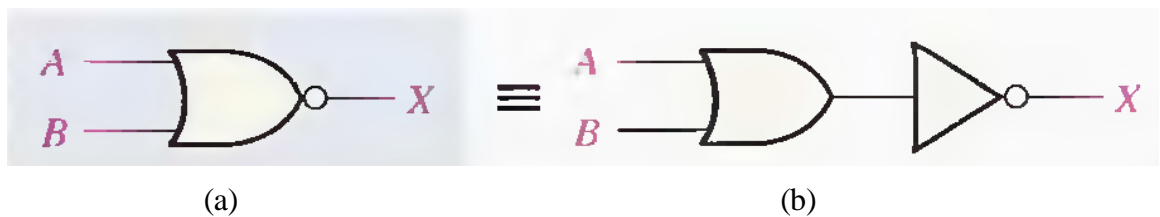

(a)   (b)

Fig.(2-14) Standard NOR gate logic symbols.

Operation of a NOR Gate

A NOR gate produces a LOW output when any of its inputs is HIGH. Only when all of its inputs are LOW is the output HIGH. For the specific case of a 2-input NOR gate, as shown in Fig.(2-14) with the inputs labelled A and B and the output labelled X, the operation can be stated as follows:

For a 2-input NOR gate, output X is LOW when either input A or input B is HIGH, or when both A and B are HIGH; X is HIGH only when both A and B are LOW.

This operation results in an output level opposite that of the OR gate. In a NOR gate, the LOW output is the active or asserted output level as indicated by the bubble on the output.

Fig.(2-15) illustrates the operation of a 2-input NOR gate for all four possible input combinations, and Table 2-6 is the truth table for a 2-input NOR gate.
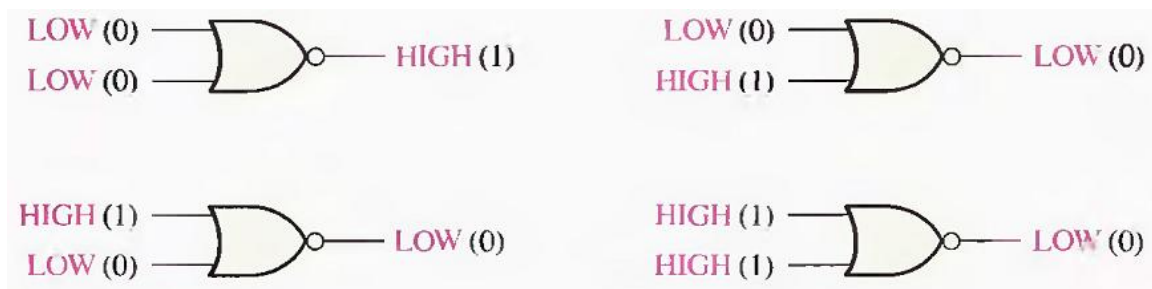
Fig.(2-15) Operation of a 2-input NOR gate.

Table 2-6 Truth table for a 2-input NOR gate.

INPUTS		OUTPUT
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

1 = HIGH, 0 = LOW.

Negative-AND Equivalent Operation of the NOR Gate

A NOR gate, like the NAND, has another aspect of its operation that is inherent in the way it logically functions. Table 2-6 shows that a HIGH is produced on the gate output only when all of the inputs are LOW. From this viewpoint, a NOR gate can be used for an AND operation that requires all LOW inputs to produce a HIGH output. This aspect of NOR operation is called negative-AND.

For a 2-input NOR gate performing a negative-AND operation, output X is HIGH only when both inputs A and B are LOW.

When a NOR gate is used to detect all LOWs on its inputs rather than one or more HIGHs, it is performing the negative-AND operation and is represented by the standard symbol in Fig.(2-16). It is important to remember that the two symbols in Fig.(2-16), represent the same physical gate and serve only to distinguish between the two modes of its operation.
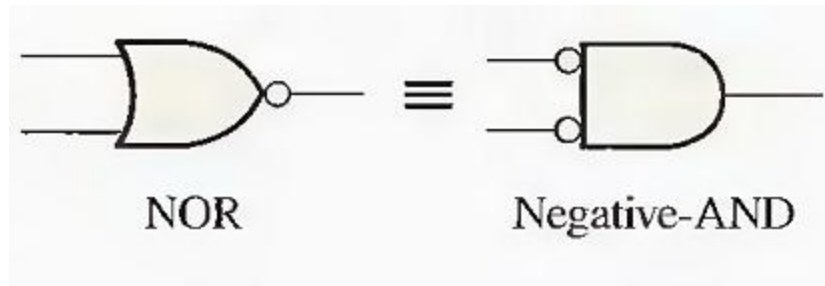
Fig.(2-16) Standard symbols representing the two equivalent operations of a NOR gate.

Logic Expressions for a NOR Gate

The Boolean expression for the output of a 2-input NOR gate can be written as

$$X = \overline{A+B}$$

This equation says that the two input variables are first ORed and then complemented, as indicated by the bar over the OR expression. Evaluating this expression, you get the results shown in Table 2-7. The NOR expression can be extended to more than two input variables by including additional letters to represent the other variables.

Table 2-7

A	B	$\overline{A+B}=X$
0	0	$\overline{0 + 0} = \overline{0} = 1$
0	1	$\overline{0 + 1} = \overline{1} = 0$
1	0	$\overline{1 + 0} = \overline{1} = 0$
1	1	$\overline{1 + 1} = \overline{1} = 0$

THE EXCLUSIVE-OR AND EXCLUSIVE-NOR GATES

Exclusive-OR and exclusive-NOR gates are formed by a combination of other gates already discussed. However, because of their fundamental importance in many applications, these gates are often treated as basic logic elements with their own unique symbols.

The Exclusive-OR Gate

Standard symbol for an exclusive-OR (XOR for short) gate is shown in Fig.(2-17). The XOR gate has only two inputs.
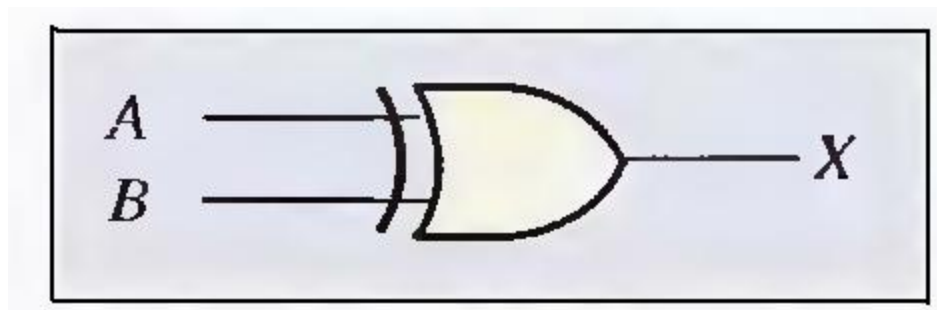

Fig.(2-17) Standard symbol for an exclusive-OR.

For an exclusive-OR gate, output X is HIGH when the two inputs are different.

The four possible input combinations and the resulting outputs for an XOR gate are illustrated in Fig.(2-18). The HIGH level is the active or asserted output level and occurs only when the inputs are at opposite levels. The operation of an XOR gate is summarized in the table shown in Table 2-8.
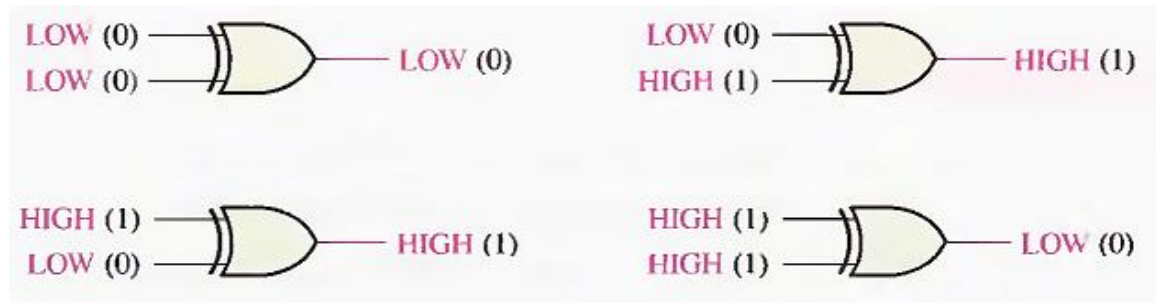
Fig.(2-18) All possible logic levels for an exclusive-OR gate.

Table 2-8 Truth table for an exclusive-OR gate.

INPUTS		OUTPUT
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

The Exclusive-NOR Gate

Standard symbols for an exclusive-NOR (XNOR) gate are shown in Fig.(2-19). Like the XOR gate, an XNOR has only two inputs. The bubble on the output of the XNOR symbol indicates that its output is opposite that of the XOR gate. When the two input logic levels are opposite, the output of the exclusive-NOR gate is LOW. The operation can be stated as follows (A and B are inputs, X is the output):

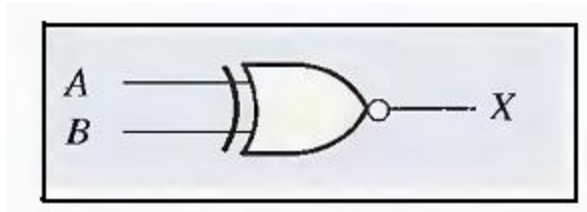**For an exclusive-NOR gate, X is HIGH only when A and B are both HIGH or both LOW.**

Fig.(2-19) Standard logic symbols for the exclusive-NOR gate.

The four possible input combinations and the resulting outputs for an XNOR gate are shown in Fig,(2-20). The operation of an XNOR gate is summarized in Table 2-9. Notice that the output is HIGH when the same level is on both inputs.
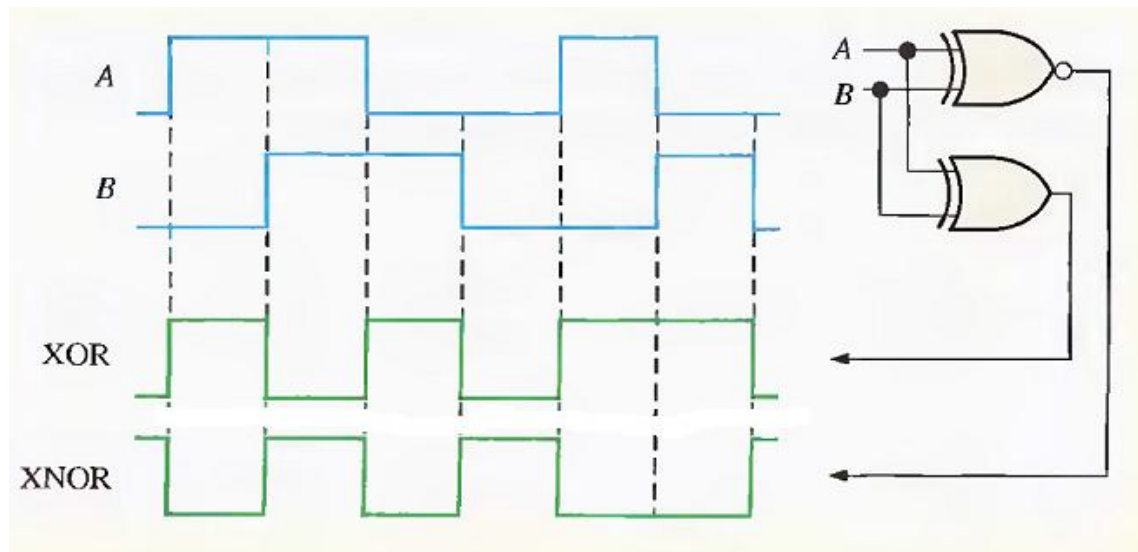

Fig.(2-20) All possible logic levels for an exclusive-NOR gate.

Table 2-9 Truth table for an exclusive-NOR gate.

INPUTS		OUTPUT
A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

Example: Determine the output waveforms for the XOR gate and for the XNOR gate, given the input waveforms, A and B, in Figure below:

GENERAL QUESTIONS

Q1: *Two electrical signals represented by A = 101101 and B = 110101 are applied to a 2-input AND gate. Sketch the output signal and the binary number it represents.*

Q2: Sketch the output waveform for a 3-input NOR gate shown in Figure below. Showing the proper time relationship to the inputs.

Finish