جمهورية العراق
وزارة التعليم العالي والبحث العلمي
جهاز الاشراف والتقويم العلمي

الجامعة : التكنولوجية
الكلية : قسم هندسة السيطرة والنظم
القسم : فرع هندسة الحاسوب
المرحلة : الرابعة
اسم المحاضر الثلاثي :صبا محمد شريف الخياط
اللقب العلمي : مدرس
المؤهل العلمي : دكتوراه هندسة الحاسوب
مكان العمل : الجامعة التكنولوجية

جدول الدروس الاسبوعي

الاسم	**د. صبا محمد شريف الخياط**
البريد الالكتروني	**siba_sharef@yahoo.com**
اسم المادة	**معمارية الحواسيب المتقدمة**
مقرر الفصل	
اهداف المادة	To study Advanced Computers Architectures, Parallel processing, and Pipelined Computers
التفاصيل الاساسية للمادة	• Introduction to super computer / super computing • Memory systems • Pipelining • Vectorization and vector processing: • Matrix operations: • Array processor • Examples of static pipelined system & vector processor
الكتب المنهجية	
المصادر الخارجية	"The Architecture of Pipelined Computers"; by: Peter M. Kogge. "Computer Architecture and Parallel Processing"; by: Kai Hwang.

تقديرات الفصل	**الفصل الدراسي**	**المختبر**	**الامتحانات اليومية**	**المشروع**	**الامتحان النهائي**
	%20	**---**	**%10**	**---**	**%70**

معلومات اضافية	

جمهورية العراق

وزارة التعليم العالي والبحث العلمي

جهاز الاشراف والتقويم العلمي

الجامعة :

الكلية :

اسم القسم :

المرحلة :

اسم المحاضر الثلاثي:

اللقب العلمي :

المؤهل العلمي :

جدول الدروس الاسبوعي

الاسبوع	التاريخ	المادة النظرية	المادة العلمية	الملاحظات
1	22/9	**Introduction to Advanced computer architecture**		
2	29/9	**Parallelism in uniprocessor system** Multiplicity of functional units, Parallelism and pipelining within the CPU, Overlapped CPU and I/O operations		
3	6/10	**Parallelism in uniprocessor system** Use of hierarchical memory system, Balancing of subsystem bandwidths, Multiprogramming and Timesharing		
4	13/10	Main structures of SISD, SIMD, MISD, MIMD		
5	20/10	ALU : carry propagate adder CPA, carry look ahead adder CLA.		
6	27/10	CSA, I/O techniques.		
7	3/11	Comparison between parallelism and pipelining		
8	10/11	Parallel adders, parallel Multipliers		
9	17/11	**Memory systems:** Organization, interleaving (high order, low order)		
10	24/11	**Memory systems** Local memory types		
11	1/12	**Pipelining :** General principles		
12	8/12	**Pipelining :** Arithmetic pipeline, design example- pipeline adder.		

		Pipelining : Instruction pipeline, data dependency, branch instruction problems.	**15/12**	**13**
		Pipeline hard ware design: Buffering, logic stage, data control, timing operation.	**22/12**	**14**
		Pipeline analysis (timing, control): Reservation table, states.	**29/12**	**15**
				16
		عطلة نصف السنة		
		Pipeline analysis (timing, control): Collision & collision vector analysis, hardware initiation.	**16/2**	**17**
		Pipeline analysis (timing, control): State diagram, Modified state diagram	**23/2**	**18**
		Pipeline analysis (timing, control): Micro-programmed pipeline.	**2/3**	**19**
		Vector processing: Vector instruction, vector processor.	**9/3**	**20**
		Vector processing: Typical Hardware architecture	**16/3**	**21**
		User Interface- the machine level instruction architecture Opcode, operand specification	**23/3**	**22**
		User Interface- the machine level instruction architecture Status and sequencing, other architectural considerations	**30/3**	**23**
		Vector Addressing Modes Dense/regular, Sparse	**6/4**	**24**
		Matrix operations: Row, Column, sub-matrix Addressing.	**13/4**	**25**
		Array processor : Architecture, switching, alignment circuits.	**20/4**	**26**
		Array processor : Topology analysis (Mesh, barrel Networks.)	**27/4**	**27**
		Sample systems of static pipelined system & vector processor: IBM 2938 array processor.	**4/5**	**28**
		Sample systems of static pipelined system & vector processor: The Texas instrument advanced scientific computer.	**11/5**	**29**
		Sample systems of static pipelined system & vector processor: Control Data STAR-100 computer.	**18/5**	**30**
		Sample systems of static pipelined system & vector processor: IBM 3838 array processor.	**25/5**	**31**
		Final exams	**1/6**	**32**

توقيع الاستاذ : توقيع العميد :

Republic of Iraq
The Ministry of Higher Education
& Scientific Research

University:UOT
College:Control &nSystems
Department: Computer Eng.
Stage: 4
Lecturer name:Siba M. Sharef
Academic Status:Lecturer
Qualification:PhD
Place of work:UOT

Course Weekly Outline

Course Instructor	Dr. Siba Mohammed Sharef				
E_mail	siba_sharef@yahoo.com				
Title	Advanced Computer Architecture				
Course Coordinator					
Course Objective	To study Advanced Computers Architectures, Parallel processing, and Pipelined Computers				
Course Description	• Introduction to super computer / super computing • Memory systems • Pipelining • Vectorization and vector processing: • Matrix operations: • Array processor • Examples of static pipelined system & vector processor				
Textbook					
References	"The Architecture of Pipelined Computers"; by: Peter M. Kogge. "Computer Architecture and Parallel Processing"; by: Kai Hwang.				
Course Assessment	Term Tests	Laboratory	Quizzes	Project	Final Exam
	20%	----	10%	----	70%
General Notes					

Republic of Iraq
The Ministry of Higher Education
& Scientific Research

University:
College:
Department:
Stage:
Lecturer name:
Academic Status:
Qualification:
Place of work:

Course weekly Outline

Week	Date	Topics Covered	Lab. Experiment Assignments	Notes
1	**22/9**	**Introduction to Advanced computer architecture**		
2	**29/9**	**Parallelism in uniprocessor system** Multiplicity of functional units, Parallelism and pipelining within the CPU, Overlapped CPU and I/O operations		
3	**6/10**	**Parallelism in uniprocessor system** Use of hierarchical memory system, Balancing of subsystem bandwidths, Multiprogramming and Timesharing		
4	**13/10**	Main structures of SISD, SIMD, MISD, MIMD		
5	**20/10**	ALU : carry propagate adder CPA, carry look ahead adder CLA.		
6	**27/10**	CSA, I/O techniques.		
7	**3/11**	Comparison between parallelism and pipelining		
8	**10/11**	Parallel adders, parallel Multipliers		
9	**17/11**	**Memory systems:** Organization, interleaving (high order, low order)		
10	**24/11**	**Memory systems** Local memory types		
11	**1/12**	**Pipelining :** General principles		
12	**8/12**	**Pipelining :** Arithmetic pipeline, design example-pipeline adder.		
13	**15/12**	**Pipelining :** Instruction pipeline, data dependency, branch instruction problems.		
14	**22/12**	**Pipeline hard ware design:** Buffering, logic stage, data control, timing operation.		
15	**29/12**	**Pipeline analysis (timing, control):**		

		Reservation table, states.		
16				
Half-year Break				
17	**16/2**	**Pipeline analysis (timing, control):** Collision & collision vector analysis, hardware initiation.		
18	**23/2**	**Pipeline analysis (timing, control):** State diagram, Modified state diagram		
19	**2/3**	**Pipeline analysis (timing, control):** Micro-programmed pipeline.		
20	**9/3**	**Vector processing:** Vector instruction, vector processor.		
21	**16/3**	**Vector processing:** Typical Hardware architecture		
22	**23/3**	**User Interface- the machine level instruction architecture** Opcode, operand specification		
23	**30/3**	**User Interface- the machine level instruction architecture** Status and sequencing, other architectural considerations		
24	**6/4**	**Vector Addressing Modes** Dense/regular, Sparse		
25	**13/4**	**Matrix operations:** Row, Column, sub-matrix Addressing.		
26	**20/4**	**Array processor :** Architecture, switching, alignment circuits.		
27	**27/4**	**Array processor :** Topology analysis (Mesh, barrel Networks.)		
28	**4/5**	**Sample systems of static pipelined system & vector processor:** IBM 2938 array processor.		
29	**11/5**	**Sample systems of static pipelined system & vector processor:** The Texas instrument advanced scientific computer.		
30	**18/5**	**Sample systems of static pipelined system & vector processor:** Control Data STAR-100 computer.		
31	**25/5**	**Sample systems of static pipelined system & vector processor:** IBM 3838 array processor.		
32	**1/6**			

Instructor Signature: **Dean Signature:**