University of Technology

Department of Computer Sciences

Final Examination 2011-2012

Subject: logic design
year:2011/1012
Division: software and information system *Time:3 hours*
Examiner: Enas tariq
Date:29/5/1012
Answer (five) Question Only

Note:10 mark for all question

Q1/ Draw 4-bit parallel adder find the sum and output carry for the addition of the following input carry $C_{n-1} = 1$.
$A_4A_3A_2A_1 = 1101$ *and* $B_4B_3B_2B_1 = 1001$

Q2/ Implement a full adder with a decoder and tow or Gates
S(x,y,z)=∑(1,2,4,7)
C(x,y,z)=∑(3,5,6,7)
3-to-8 line decoder

Q3/ Design 1-to-8 Demultiplexer

Q4/ What is the type of shift Register, and Design shift register 4-bit.

Q5/

1. Use K-map to simplify the following expression:
   F(A,B,C,D)=Σ0,3,4,7,8without don't care
   F(A,B,C,D)=Σ12,13,14,10,11witht don't care
2- Simplify the following Boolean expression with drawing before and after simplified.

AB+A(B+C)+B(B+C)

Q6/Answer all question below

1- Convert Decimal to Hexadecimal (650).
2- Convert BCD number to Gray (0100).
3- Addition Hexadecimal (3BC) + (428).
4-find the 1's and 2's complement of binary number (10110010)
5-Subtract Octal number (45) + (14).