

**University of Technology**  
**Computer Engineering Department**  
**Logic Design Laboratory**

Digital logic devices are the circuits that electronically perform logic operations on binary variables. The binary information is represented by high and low voltage levels, which device processes electronically. The devices that perform the simplest of the logic operations (such as AND, OR, NAND, etc.) are called gates. This laboratory contains these experiments.

| <b>Exp. No.</b> | <b>Exp. Title</b>   | <b>Time</b> |
|-----------------|---|-------------|
|                 | <b>Introduction</b>                                       | <b>2</b>    |
| <b>1</b>        | <b>Introduction to combinational design</b>               | <b>2</b>    |
| <b>Part 1</b>   | <b>AND Gate &amp; It's Application</b>                    | <b>2</b>    |
| <b>Part 2</b>   | <b>OR Gate &amp; It's Application</b>                     | <b>2</b>    |
| <b>Part 3</b>   | <b>Exclusive OR Gate &amp; It's Application</b>           | <b>2</b>    |
| <b>2</b>        | <b>Universal gates<br/>NAND Gate</b>                      | <b>2</b>    |
| <b>Part 1</b>   | <b>Implementing inverter using NAND Gate</b>              | <b>2</b>    |
| <b>Part 2</b>   | <b>NOR Gate</b>   | <b>2</b>    |
| <b>Part 3</b>   | <b>Implementing inverter using NOR Gate</b>               | <b>2</b>    |
|                 |   | <b>2</b>    |
| <b>3</b>        | <b>Implementing combinational circuits</b>                | <b>2</b>    |
| <b>4</b>        | <b>Implementation of half adder</b>                       | <b>2</b>    |
| <b>Part 1</b>   | <b>Implementation of full adder</b>                       | <b>2</b>    |
| <b>5</b>        | <b>Designing BCD-to-seven segment decoder</b>             | <b>2</b>    |
| <b>6</b>        | <b>Decoder</b>  | <b>2</b>    |
| <b>7</b>        | <b>Multiplexer</b>  | <b>2</b>    |
| <b>Part 1</b>   | <b>Implementing of Boolean function using Multiplexer</b> | <b>2</b>    |
| <b>Part 2</b>   | <b>Demultiplexer</b>                                      | <b>2</b>    |
| <b>8</b>        | <b>Flip-Flops<br/>The set –Rest (S-R) flip-flop</b>       | <b>2</b>    |

|               |  |          |
|---------------|--|----------|
|               | <b>The clocked set –Rest (S-R) flip-flop</b>       |          |
| <b>Part 1</b> | <b>The J-K flip-flop<br/>The D-Type Flip-flop</b>  | <b>2</b> |
| <b>Part 2</b> | <b>The T-type Flip-flop</b>                        | <b>2</b> |
| <b>9</b>      | <b>The Shift Registers &amp; There Application</b> | <b>2</b> |
| <b>10</b>     | <b>Digital Counters<br/>Decade Counter</b>         | <b>2</b> |
| <b>Part 1</b> | <b>Up-Down Counter</b>                             | <b>2</b> |