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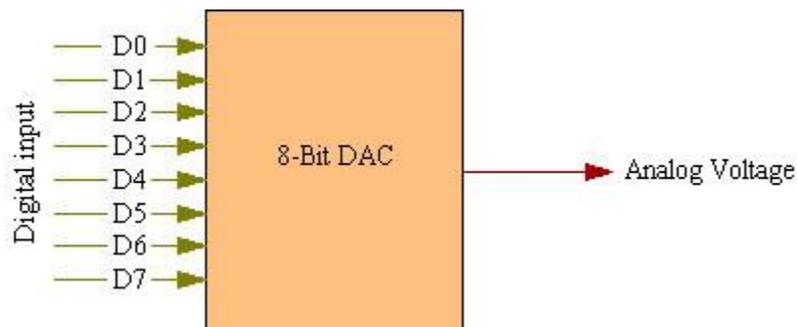
Digital to Analog converters

OBJECT:-

To Interface Digital -to-Analog converter to 8085 using 8255 and write Assembly Language Program to generate Ramp Wave form.

THEORY:-

Digital-to-Analog Conversion or simply DAC, is a device that is used to convert a digital (usually binary) code into an analog signal (current, voltage, or electric charge). Digital-to-analog conversion is the primary means by which digital equipment such as computer-based systems are able to translate digital data into real-world signals that are more understandable to or useable by humans, such as music, speech, pictures, video. It also allows digital control of machines, equipment, household appliances. When data is in binary form, the 0's and 1's may be of several forms such as the TTL form where the logic zero may be a value up to 0.8 volts and the 1 may be a voltage from 2 to 5 volts. The data can be converted to clean digital form using gates which are designed to be on or off depending on the value of the incoming signal. Data in clean binary digital form can be converted to an analog form by using a summing amplifier. Here is a simplified functional diagram of an 8-bit DAC.



There are mainly two techniques used for digital to analog conversion

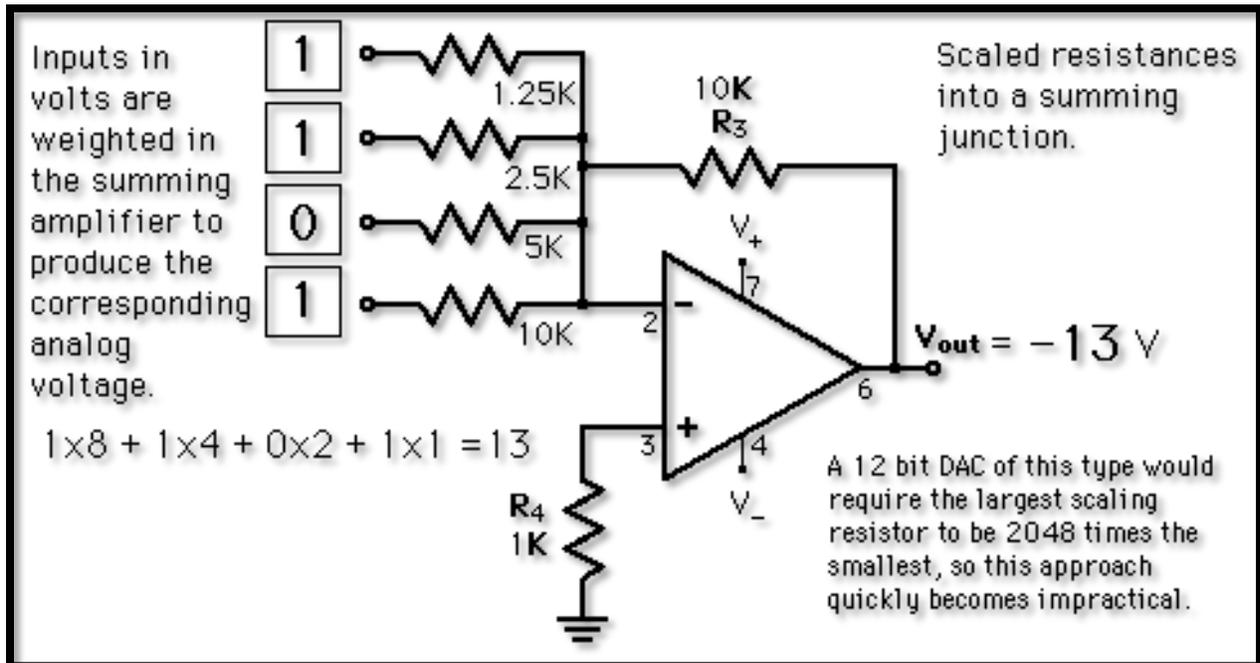
1. **Weighted Summing Amplifier**
2. **R-2R Network Approach**

Weighted Sum DAC

One way to achieve D/A conversion is to use a summing amplifier.

This approach is not satisfactory for a large number of bits because it requires too much precision in the summing resistors.

This problem is overcome in the R-2R network DAC.

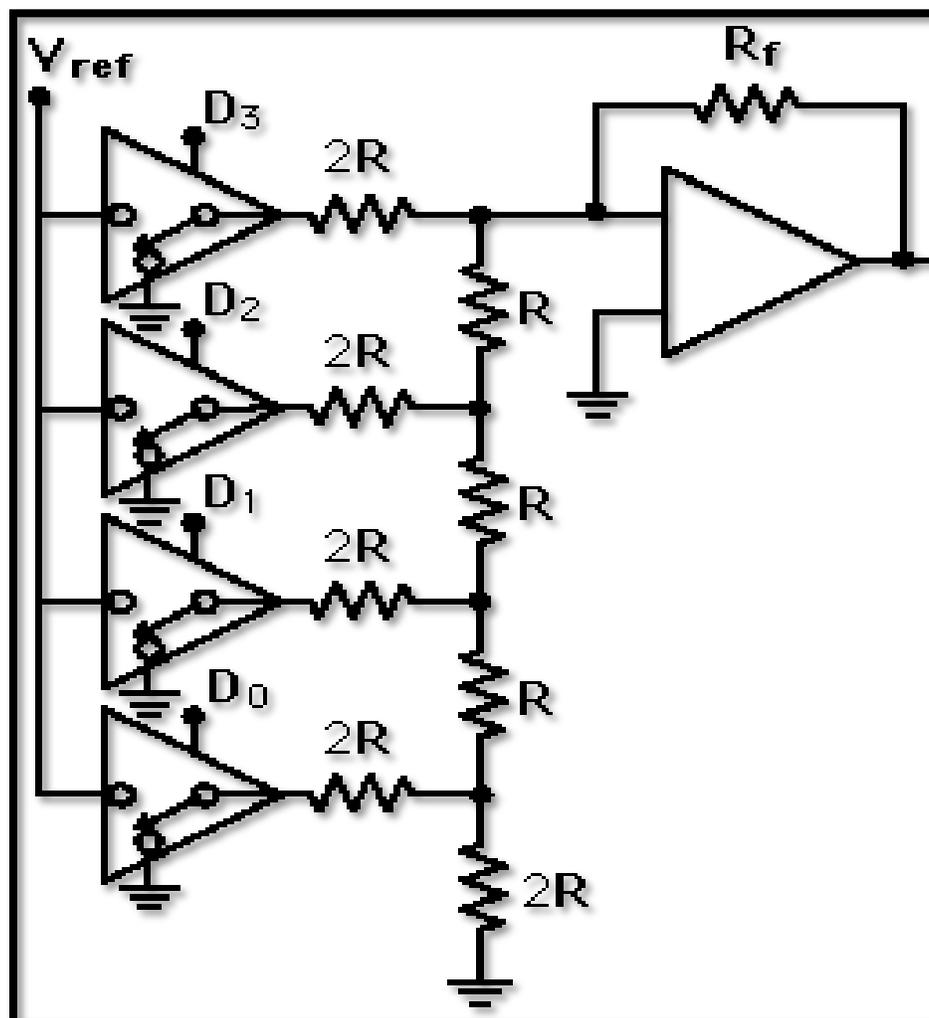


R-2R Ladder DAC

The summing amplifier with the R-2R ladder of resistances shown produces the output where the D's take the value 0 or 1.

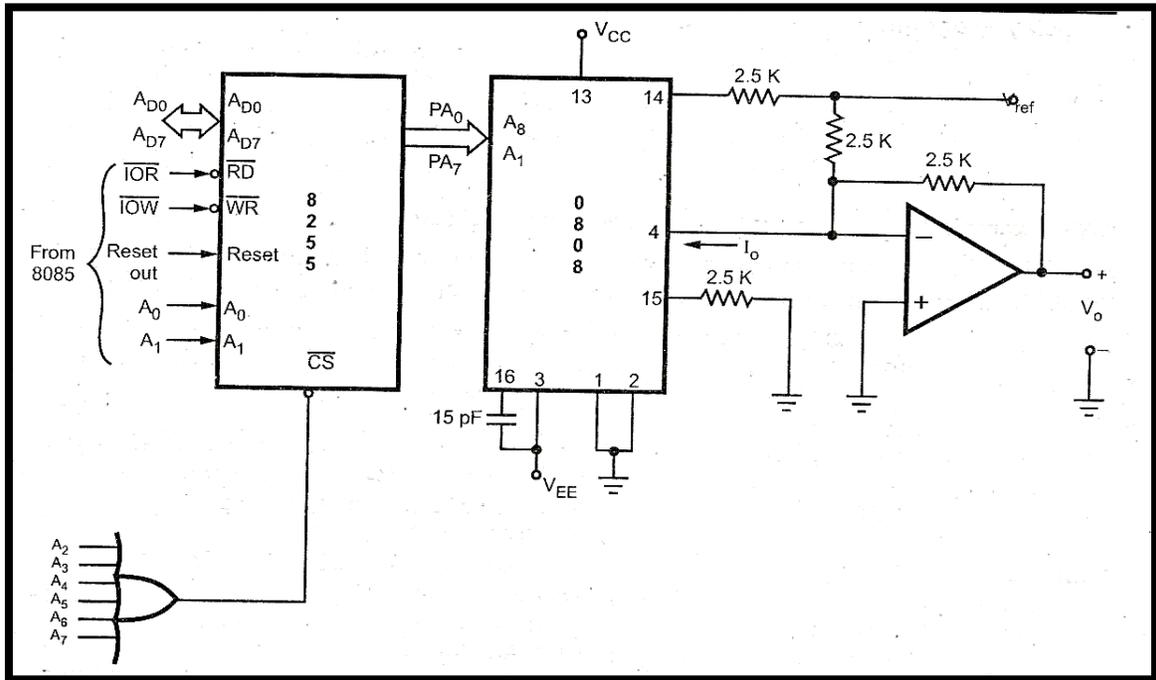
The digital inputs could be TTL voltages which close the switches on a logical 1 and leave it grounded for a logical 0.

This is illustrated for 4 bits, but can be extended to any number with just the resistance values R and 2R.



$$V_{out} = \frac{R_f}{R} V_{ref} \left[\frac{D_0}{16} + \frac{D_1}{8} + \frac{D_2}{4} + \frac{D_3}{2} \right]$$

The interfacing of DAC 0808 with microprocessor 8085 is shown below. Here, programmable peripheral interface, 8255 is used as parallel port to send the digital data to DAC.



Interfacing Digital-To-Analog converter to 8085 using 8255

Figure below shows the interfacing of DAC 0808 with microprocessor 8085. Here, programmable peripheral interface, 8255 is used as parallel port to send the digital data to DAC.

I/O Map for 8255

Port/Register	Address
Port A	00
Port B	01
Port C	02
Control Register	03

Program:

```
MVI A, 80H ; Initialization -control word for 8255 to Configure all ports as output ports
OUT 03

MVI A, DATA ; Load 8-bit data to be sent at the input of 0808 DAC
OUT 00 ; Send data on port A.
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A Circuit Description of DAC module

When chip select of DAC is enabled then DAC will convert digital input value given through portlines PB0-PB7 to analog value. The analog output from DAC is a current quantity. This current is converted to voltage using OPAMP based current-to-voltage converter. The voltage outputs (+/- 8V for bipolar 0 to 8V for unipolar mode) of OPAMP are connected to CRO to see the wave form. Port A & Port B are connected to channel 1 and channel 2 respectively. A reference voltage of 8V is generated using 723 and is given to Verify points of the DAC 0800. The standard output voltage will be 7.98V when FF is outputted and will be 0V when 00 is outputted. The Output of DAC-0800 is fed to the operational amplifier to get the final output as **X OUT** and **YOUT**.

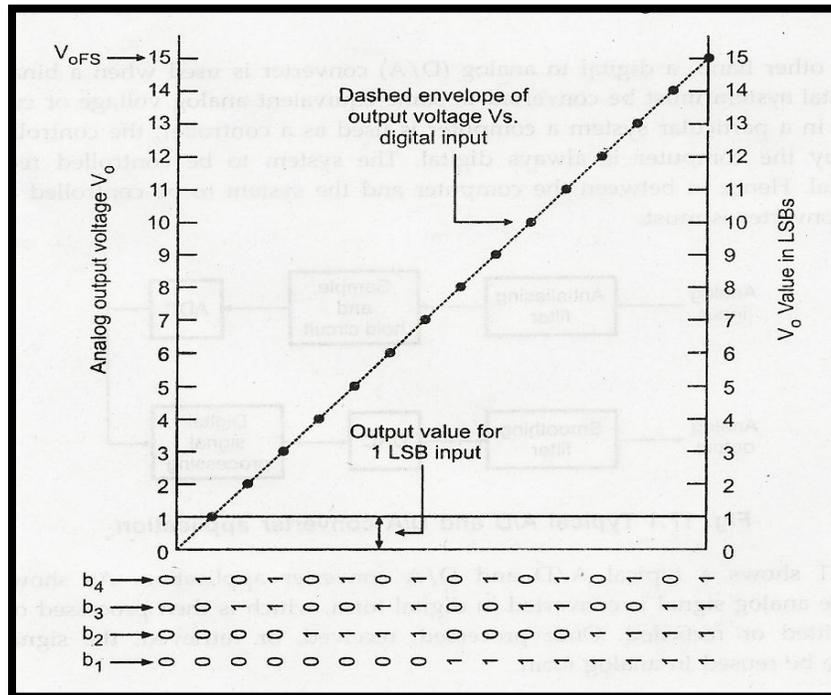


Figure shows analog output voltage v_o is plotted against all 16 possible digital input words.

Performance Parameters of DAC:

The performance parameters of DAC are:

1. Resolution

Resolution is defined in two ways.

- o Resolution is the number of different analog output values that can be provided by a DAC. For an n-bit DAC

$$\text{Resolution} = 2^n \dots\dots\dots (1)$$

- o Resolution is also defined as the ratio of a change in output voltage resulting from a change of 1 LSB at the digital inputs. For an n-bit DAC it can be given as:

$$\text{Resolution} = \text{VoFs} / 2^n - 1 \dots\dots\dots(2)$$

Where, VoFs = Full scale output voltage

From equation(1), we can say that, the resolution can be determined by the number of bits in the input binary word. For an 8-bit resolution can be given as

$$\text{resolution} = 2^n = 2^8 = 256$$

If the full scale output voltage is 10.2 V then by second definition the resolution for an 8-bit can be given as

$$\begin{aligned} \text{Resolution} = \text{VoFs} / 2^n - 1 &= 10.2 / 2^8 - 1 = 10.2 / 255 \\ &= 40 \text{ mV/LSB} \end{aligned}$$

Therefore, we can say that an input change of 1 LSB causes the output to change by 40 mv

2. Accuracy

It is a comparison of actual output voltage with expected output. It is expressed in percentage. Ideally, the accuracy of DAC should be, at worst, $\pm 1/2$, of its LSB. If the full scale output voltage is 10.2 V then for an 8-bit DAC accuracy can be given as

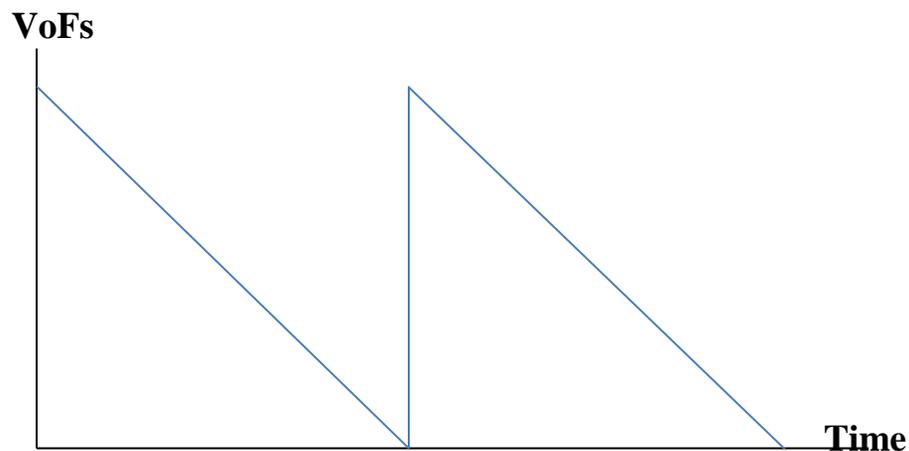
$$\begin{aligned} \text{Accuracy} &= \text{VoFs} / (2^n - 1)_2 \\ &= 10.2 / 255 \times 2 = 20 \text{ mV} \end{aligned}$$

PROCEDURE:-

1. Connect power supply 8V & GND to both microprocessor trainer kit & DAC interfacing kit.
2. Connect data bus between microprocessor trainer kit & DAC interfacing kit.
3. Enter the program to generate Ramp Wave.
4. Execute your program from respective locations and observe the waveform on oscilloscope.

HOME WORK

- **An 8 bit DAC has an output voltage range of 0 – 2.55 V. Define its resolution in two ways.**
- **A 12-bit DAC has a step size of 8 mv. Determine the full scale output voltage and percentage resolution.**
- **Write a program to output this signal**



Programmable Peripheral Interface-8255:-

The 8255 is a general purpose programmable I/O device used for parallel data transfer. It has 24 I/O pins which can be grouped in three 8-bit parallel ports: Port A, Port B and Port C. The eight bits of port C can be used as individual bits or be grouped in two 4-bit ports: Copper (C_u) and C lower, (CL).

The 8255, primarily, can be programmed in two basic modes Bit Set/Reset (BSR) mode and I/O mode. The BSR mode is used to set or reset the bits in port C.

The I/O mode is further divided into three modes:

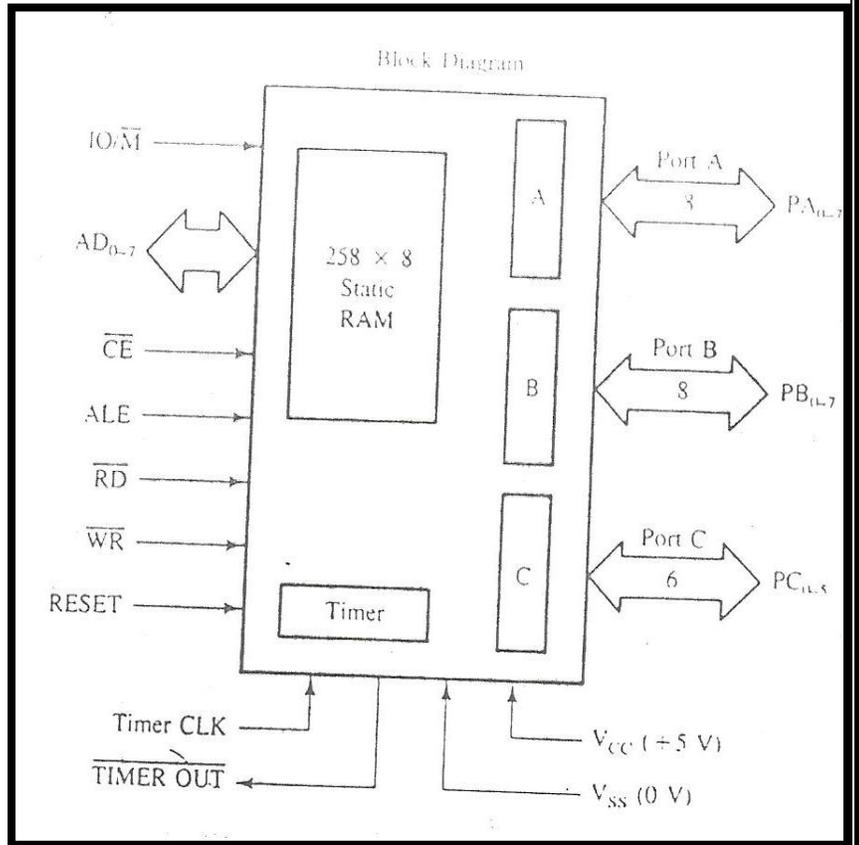
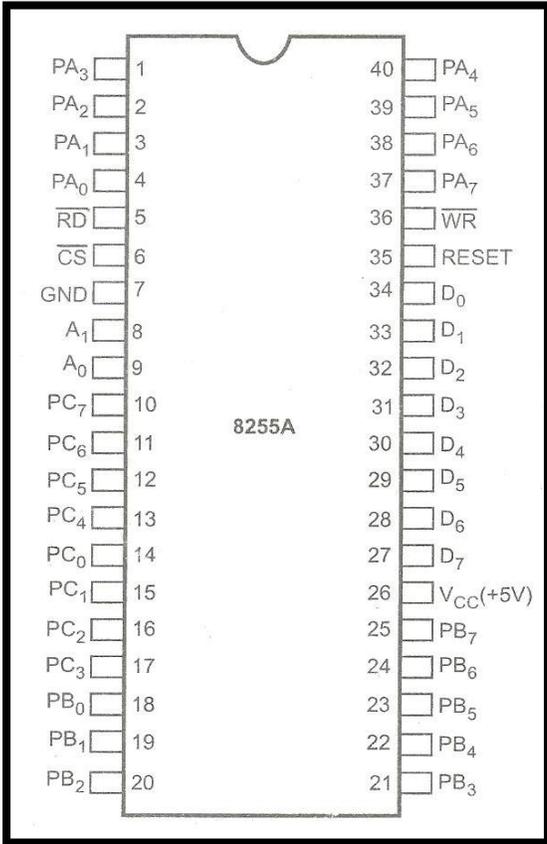
Mode0: Simple Input/output.

Mode1: Input/output with handshake.

Mode2: Bi-directional I/O data transfer.

The function of I/O pins (input or output) and modes of operation of I/O ports can be programmed by writing proper control word in the control word register. Each bit in the control word has a specific meaning and the status of these bits decides the function and operating mode of the I/O ports.

PIN Diagram:



Pin Symbols	Function
D ₀ -D ₇ (Data Bus)	These bi-directional, tri-state data bus lines are connected to the system data bus. They are used to transfer data and control word from microprocessor (8085) to 8255 or to receive data or status word from 8255 to the 8085.
PA ₀ -PA ₇ (Port A)	These 8-bit bi-directional I/O pins are used to send data to output device and to receive data from input device. It functions as an 8-bit data output latch/buffer, when used in output mode and an 8-bit data input buffer, when used in input mode.
PB ₀ -PB ₇ (Port B)	These 8-bit bi-directional I/O pins are used to send data to output device and to receive data from input device. It functions as an 8-bit data, output latch/buffer when used in output mode and an 8-bit data input buffer, when used in input mode.
PC ₀ -PC ₇	These 8-bit bi-directional I/O pins are divided into two groups PC _L (PC ₃ -PC ₀) and PC _U (PC ₇ -PC ₄). These groups individually can transfer data in or out when programmed for simple I/O, and used as handshake signals when programmed for handshake or bi-directional modes.
$\overline{\text{RD}}$ (Read)	When this pin is low, the CPU can read the data in the ports or the status word, through the data buffer.
$\overline{\text{WR}}$ (Write)	When this input pin is low, the CPU can write data on the ports or in the control register through the data bus buffer.
$\overline{\text{CS}}$ (Chip Select)	This is an active low input which can be enabled for data transfer operation between the CPU and the 8255.
RESET	This is an active high input used to reset 8255. When RESET input is high, the control register is cleared and all the ports are set to the input mode. Usually RESET.OUT signal from 8085 is used to reset 8255.
A ₀ and A ₁	These input signals along with $\overline{\text{RD}}$ and $\overline{\text{WR}}$ inputs control the selection of the control/status word registers or one of the three ports. Table. 12.15 summarizes the status of A ₀ , A ₁ , $\overline{\text{CS}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ to access the control word/ports. A ₀ and A ₁ are generally connected to the A ₀ , A ₁ pins of the address bus; the 8255 therefore occupies four consecutive locations in the I/O space.

For I/O Mode

The mode definition format for I/O mode is shown in Figure below. The control words for both, mode definition and Bit Set-Reset are loaded into the same control register, with bit D7 used for specifying whether the word loaded into the control register is a mode definition word or Bit Set-Reset word. If D7 is high, the word is taken as a mode definition word, and if it is low, it is taken as a Bit Set-Reset word. The appropriate bits are set or reset depending on the type of operation desired, and loaded into the control register.

