**8-FET DC Biasing**

The general relationships that can be applied to the dc analysis of all FET amplifiers:

\[ I_D = 0 \text{ A} \]  
\[ I_D = I_S \]  
\[ I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 \]  
\[ I_D = k(V_{GS} - V_T)^2 \]

JFET & D-MOSFET, Shockley's equation is applied to relate the input & output quantities:

\[ I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 \]

For enhancement-type MOSFETs, the following equation is applicable:

\[ I_D = k(V_{GS} - V_T)^2 \]

**Fixed-Bias Configuration**

Replacing \( R_G \) by a short-circuit equivalent, as in fig8-2, Applying KVL will result:

\[ -V_{GG} - V_{GS} = 0 \]

Since \( V_{GG} \) is a fixed dc supply, \( V_{GS} \) is fixed in magnitude

\[ I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 \]

The fixed level of \( V_{GS} \) has been superimposed as a vertical line at \( V_{GS} = -V_{GG} \). \( I_D \) determined at any point on the vertical line (\( V_{GS} = -V_{GG} \)).

**Fig8-1 Fixed-Bias Configuration**

**Fig8-2 Network for DC analysis**

\[ V_{in} = I_C R_G = (0 \text{ A}) R_G = 0 \text{ V} \]

**Fig8-3 plotting Shockely's equation**

**Fig8-4 solution for the fixed bias configuration**
Example 1: Determine the following for the network of fig 8-5, (a) $V_{GSQ}$ (b) $I_{DQ}$ (c) $V_{DS}$ (d) $V_D$ (e) $V_G$ (f) $V_S$

Solution:
From the graph of fig 8-6, 5.6 mA is quite acceptable. Therefore, for part (a)

$$V_{GSQ} = -V_{GG} = -2 \text{ V}$$

(b) $I_D = 5.6 \text{ mA}$

(c) $V_{DS} = V_{DD} - I_D R_D = 16 \text{ V} - (5.6 \text{ mA})(2 \text{ k}\Omega)$

$$= 16 \text{ V} - 11.2 \text{ V} = 4.8 \text{ V}$$

(d) $V_D = V_{DS} = 4.8 \text{ V}$

(e) $V_G = V_{GS} = -2 \text{ V}$

(f) $V_S = 0 \text{ V}$

Self-Bias Configuration
The controlling gate-to-source voltage is now determined by the voltage across a resistor $R_S$ introduced in the source leg of the configuration in fig 8-7
The current through $R_S$ is the source current $I_S$ but $I_S = I_D$ and

$$V_{R_S} = I_D R_S$$

For the indicated closed loop of fig 8-8 we find that

$$-V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = -V_{R_S}$$

or

$$V_{GS} = -I_D R_S$$

Substituting this equation into Shockley’s equation as below:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$= I_{DSS} \left(1 - \frac{-I_D R_S}{V_p}\right)^2$$

$$I_D = I_{DSS} \left(1 + \frac{I_D R_S}{V_p}\right)^2$$

so we must identify two point, the first point as defines shown in fig8-9, the second point identifies by using this approximating:

$$I_D = \frac{I_{DSS}}{2}$$

Then

$$V_{GS} = -I_D R_S = -\frac{I_{DSS} R_S}{2}$$

Applying KVL to the output circuit to determine the $V_{DS}$

$$V_{Rs} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and

$$V_{DS} = V_{DD} - V_{Rs} - V_{R_D} = V_{DD} - I_S R_S - I_D R_D$$
Example 2: Determine the following for the network of fig8-11, (a) $V_{GSQ}$ (b) $I_{DQ}$ (c) $V_{DS}$ (d) $V_S$ (e) $V_G$ (f) $V_D$

Solution:

Choosing $I_D = 4mA$, we obtain

$$V_{GS} = -I_D R_S$$

Choosing $I_D = 4mA$, we find

$$V_{GS} = -(4 mA)(1 k\Omega) = -4 V$$

The result is the plot of fig8-12 as defined by the network. If choose $V_{GS} = V_P / 2 = -3V$, we find $I_D = I_{DSS} / 4 = 8mA / 4 = 2mA$, as shown in fig 8-13

(b) At the quiescent point:

$$I_{DQ} = 2.6 mA$$

(c) Eq[8-11]:

$$V_{GSQ} = -2.6 V$$
\[ V_{DS} = V_{DD} - I_D(R_S + R_D) \]
\[ = 20 \text{ V} - (2.6 \text{ mA})(1 \text{ k}\Omega + 3.3 \text{ k}\Omega) \]
\[ = 20 \text{ V} - 11.18 \text{ V} \]
\[ = 8.82 \text{ V} \]

(d) Eq.[8-12]:

\[ = (2.6 \text{ mA})(1 \text{ k}\Omega) \]
\[ = 2.6 \text{ V} \]

(e) Eq. [8-13]:

\[ V_G = 0 \text{ V} \]

(f) Eq.[8-14]:

\[ V_D = V_{DS} + V_S = 8.82 \text{ V} + 2.6 \text{ V} = 11.42 \text{ V} \]
\[ V_D = V_{DS} - I_D R_S = 20 \text{ V} - (2.6 \text{ mA})(3.3 \text{ k}\Omega) = 11.42 \text{ V} \]

**Example 3:** Find the quiescent point for the network of fig8-11 if (a) RS=100Ω, (b) RS=10kΩ

(a) \( I_D \) scale

From Eq.[9-10]

\[ I_{DQ} = 6.4 \text{ mA} \]

\[ V_{GSQ} = -0.64 \text{ V} \]

From Eq.[9-10]

\[ I_{DQ} = 0.46 \text{ mA} \]

**Example 4:** Determine the following for the common-gate configuration of fig8-16
(a) \( V_{GSO} \) (b) \( I_D \) (c) \( V_D \) (d) \( V_G \) (e) \( V_S \) (f) \( V_{DS} \)
Solution:
a) The transfer characteristic and load line appear in fig8-18. The second point for the sketch of the load line was determined by choosing (arbitrarily) $I_D = 6\, mA$, solving for $V_{GS}$

$$V_{GS} = -I_D R_S = -(6 \, mA)(680 \, \Omega) = -4.08 \, V$$

As shown in fig8-18. The device transfer curve was sketched using

$$I_D = \frac{I_{DS}}{4} = \frac{12 \, mA}{4} = 3 \, mA$$
$$V_{GS} = \frac{V_p}{2} = -\frac{6 \, V}{2} = -3 \, V$$

The resulting quiescent point of fig8-18 is:

$$V_{GSq} = -2.6 \, V$$

(b) from fig8-18

$$I_{Dq} = 3.8 \, mA$$

(c) $V_D = V_{DD} - I_D R_D$

$$= 12 \, V - (3.8 \, mA)(1.5 \, k\Omega) = 12 \, V - 5.7 \, V = 6.3 \, V$$

(d) $V_G = 0 \, V$

(e) $V_S = I_D R_S = (3.8 \, mA)(680 \, \Omega)$

$$= 2.58 \, V$$

(f) $V_{DS} = V_D - V_S$

$$= 6.3 \, V - 2.58 \, V = 3.72 \, V$$

Voltage-Divider Biasing

---

Applying KVL in the clockwise direction to the indicated loop of fig 8-20

$$V_G - V_{GS} - V_{R_1} = 0$$

$$V_{GS} = V_G - V_{R_1}$$

$$V_{R_1} = I_S R_S = I_D R_S$$, we have

$$V_{GS} = V_G - I_S R_S$$

Set $I_D = 0mA$ resulting:
For the other point, let us now employ the fact that:

\[ V_{GS} = V_G - I_D R_S \]

Increasing values of \( R_S \) result in lower quiescent values of \( I_D \) and more negative values of \( V_{GS} \).

**Example 5:** Determine the following for the network of fig 8-23, (a) \( I_{DQ} \) & \( V_{GSQ} \) (b) \( V_D \) (c) \( V_S \) (d) \( V_{DS} \) (e) \( V_{DG} \)

**Solution:** a) For the transfer char., if \( I_D = I_{DSS}/4 = 8\text{mA}/4 = 2\text{mA} \), then \( V_{GS} = V_G/2 = -4\text{V}/2 = -2\text{V} \)

The resulting curve in fig 8-24; the network equation is defined by:
Example 5: Determine the following for the network of Fig 8-25, (a) $I_{DQ}$ & $V_{GSQ}$ (b) $V_{DS}$ (c) $V_D$ (d) $V_S$

The resulting bias line appears on Fig 8-24 with quiescent values of

$$I_{DQ} = 2.4 \text{ mA}$$
$$V_{GSQ} = -1.8 \text{ V}$$

and

(a) $V_D = V_{DD} - I_D R_D$

$$= 16 \text{ V} - (2.4 \text{ mA})(2.4 \text{ k}\Omega)$$
$$= 10.24 \text{ V}$$

(b) $V_D = V_{DD} - I_D R_D$

$$= 16 \text{ V} - (2.4 \text{ mA})(2.4 \text{ k}\Omega)$$
$$= 10.24 \text{ V}$$

(c) $V_S = I_D R_S = (2.4 \text{ mA})(1.5 \text{ k}\Omega)$

$$= 3.6 \text{ V}$$

(d) $V_{DS} = V_{DD} - I_D (R_D - R_S)$

$$= 16 \text{ V} - (2.4 \text{ mA})(2.4 \text{ k}\Omega + 1.5 \text{ k}\Omega)$$
$$= 6.64 \text{ V}$$

$$\Rightarrow V_{DS} = V_D - V_S = 10.24 \text{ V} - 3.6 \text{ V}$$

$$= 6.64 \text{ V}$$

$$V_{GS} = V_D - V_G = 10.24 \text{ V} - 1.82 \text{ V}$$
$$= 8.42 \text{ V}$$
Solution:
a) Applying KVL to the input section of the network redrawn in fig 8-26

\[-V_{GS} - I_s R_S + V_{SS} = 0\]

or

\[V_{GS} = V_{SS} - I_s R_S\]

\[I_s = I_D\]

and

\[V_{GS} = V_{SS} - I_D R_S\]

\[V_{GS} = 10 \text{V} - I_D(1.5 \text{k}\Omega)\]

For \(I_D = 0 \text{ mA}\),

\[V_{GS} = V_{SS} = 10 \text{V}\]

For \(V_{GS} = 0 \text{V}\),

\[0 = 10 \text{V} - I_D(1.5 \text{k}\Omega)\]

\[I_D = \frac{10 \text{V}}{1.5 \text{k}\Omega} = 6.67 \text{mA}\]

For the transfer char., \(V_{GS}=V_{P}/2=-3V/2=-1.5V\) and \(I_D=I_{DSS}/4=9mA/4=2.25mA\)

\[I_D = 6.9 \text{mA}\]

\[V_{GSQ} = -0.35 \text{V}\]

b) Applying KVL to the output side of fig8-26 will result

\[-V_{SS} + I_s R_S + V_{DS} + I_D R_D - V_{DD} = 0\]

Substituting \(I_s = I_D\) and rearranging gives

\[V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)\]

\[V_{DS} = 20 \text{V} + 10 \text{V} - (6.9 \text{mA})(1.8 \text{k}\Omega + 1.5 \text{k}\Omega)\]

\[= 30 \text{V} - 22.77 \text{V}\]

\[= 7.23 \text{V}\]

(c) \(V_D = V_{DD} - I_D R_D\)

\[= 20 \text{V} - (6.9 \text{mA})(1.8 \text{k}\Omega) = 20 \text{V} - 12.42 \text{V}\]

\[= 7.58 \text{V}\]

(d) \(V_{DS} = V_D - V_S\)

or \(V_S = V_D - V_{DS}\)

\[= 7.58 \text{V} - 7.23 \text{V}\]

\[= 0.35 \text{V}\]
**Depletion – Type MOSFETS**

**Example 7:** For the n-channel depletion-type of fig8-28, determine: $I_{DQ}$ & $V_{GSO}$ & $V_{DS}$

![Fig8-28 n-DMOSFET Example 7](image)

Setting $I_D = 0$ mA results in

$$V_{GS} = V_G = 1.5 \text{ V}$$

Setting $V_{GS} = 0$ V yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5 \text{ V}}{750 \Omega} = 2 \text{ mA}$$

**Solution:** For the transfer char, $V_{GS}=V_P/2=-3V/2=-1.5$V and $I_D=I_{DSS}/4 = 6\text{mA}/4=1.5\text{mA}$, consider the level of $V_P$ and the fact that Skockley's equation defines a curve that rises more positive. A plot point will defined at $V_{GS} = +1$V.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 6 \text{ mA}\left(1 - \frac{1 \text{ V}}{3 \text{ V}}\right)^2 = 6 \text{ mA}\left(1 + \frac{1}{3}\right)^2 = 6 \text{ mA(1.778)}$$

$$= 10.67 \text{ mA}$$

**Eq[8-15]**

$$V_G = \frac{10 \text{ M} \Omega(18 \text{ V})}{10 \text{ M} \Omega + 110 \text{ M} \Omega} = 1.5 \text{ V}$$

**Eq[8-16]**

$$V_{GS} = V_G - I_D R_S = 1.5 \text{ V} - I_D(750 \Omega)$$

The plot point and resulting bias line appear in fig8-29 the resulting operating point:

$$I_{DQ} = 3.1 \text{ mA}$$

$$V_{GSQ} = -0.8 \text{ V}$$

b) **Eq[8-19]**

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$= 18 \text{ V} - (3.1 \text{ mA})(1.8 \text{ k} \Omega + 750 \Omega)$$

$$= 10.1 \text{ V}$$

**Example 8:** Repeat Example 7: with $R_S = 150\Omega$

**Solution:** (a) The plot points are the same for the transfer curve as shown in fig8-30,

$$V_{GS} = V_G - I_D R_S = 1.5 \text{ V} - I_D(150 \Omega)$$
Setting $I_D = 0 \text{ mA}$ results in

$$V_{GS} = 1.5 \text{ V}$$

Setting $V_{GS} = 0 \text{ V}$ yields

$$I_D = \frac{V_D}{R_S} = \frac{1.5 \text{ V}}{150 \Omega} = 10 \text{ mA}$$

**b) Eq[8-19]**

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$= 18 \text{ V} - (7.6 \text{ mA})(1.8 \text{ k} \Omega + 150 \Omega)$$

**Example 9: Determine the following for the network of fig8-31, $I_DQ$, $V_{GSO}$ & $V_D$**

![Fig8-31 Example 9:](image)

**Solution:**

$$V_{GS} = -I_D R_S$$

For JFET $V_{GS}$ must be less than zero volts. Therefore no requirement to plot the transfer curves for positive values of $V_{GS}$

$$I_D = \frac{I_{DSS}}{4} = \frac{8 \text{ mA}}{4} = 2 \text{ mA}$$

and

$$V_{GS} = \frac{V_p}{2} = \frac{-8 \text{ V}}{2} = -4 \text{ V}$$

and for $V_{GS} > 0 \text{ V}$, since $V_p = -8 \text{ V}$, we will choose

$$V_{GS} = +2 \text{ V}$$

and

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2 = 8 \text{ mA} \left(1 - \left(-\frac{2 \text{ V}}{8 \text{ V}}\right)^2\right) = 12.5 \text{ mA}$$

In fig 8-32. For the network bias line, at $V_{GS}=0 \text{ V}$, $I_D=0 \text{ mA}$. Choosing $V_{GS} = -6 \text{ V}$
Example 10: Determine $V_{DS}$ for the network of fig8-33

Solution:

$V_{GS} = 0 \, V$

The resulting $Q$-point:

$I_{DQ} = 1.7 \, mA$

$V_{GSO} = -4.3 \, V$

(b) $V_D = V_{DD} - I_D R_D$

$= 20 \, V - (1.7 \, mA)(6.2 \, k\Omega)$

$= 9.46 \, V$

Enhancement-Type MOSFETs

$\begin{align*}
I_{D} &= k(V_{GS} - V_{GSO})^2 \\
I_{D(on)} &= k(V_{GSO} - V_{GSTR})^2 \\
k &= \frac{I_{D(on)}}{(V_{GSO} - V_{GSTR})^2}
\end{align*}$

Feedback Biasing Arrangement
For the output circuit,

\[ V_{DS} = V_{DD} - I_D R_D \]

Which becomes the following after substituting Eq[8-27]

\[ V_{DS} = V_{DD} - I_D R_D \]

Substituting \( I_D = 0 \) mA into Eq[8-28] gives:

\[ V_{GS} = V_{DD} | I_D = 0 \text{ mA} \]

Substituting \( V_{GS} = 0 \) mA into Eq[8-28], gives:

\[ I_D = \frac{V_{DD}}{R_D} [v_s - v_0] \]

A plot defined by Eq[8-25] and [8-28] in fig 8-37 with the resulting operation point.

**Example 11:** Determine \( I_{DO} \) and \( V_{DSQ} \) for the enhancement-type MOSFET of fig 8-38.
Solution: Two points are defined immediately as shown in fig8-39. Solving for $k$, Eq[8-26]:

$$k = \frac{I_D(\text{on})}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$

$$= \frac{6 \text{ mA}}{(8 \text{ V} - 3 \text{ V})^2} = \frac{6 \times 10^{-3}}{25} \text{ A/V}^2$$

$$= 0.24 \times 10^{-3} \text{ A/V}^2$$

For $V_{GS} = 6 \text{ V}$ (between 3 and 8 V):

$$I_D = 0.24 \times 10^{-3}(6 \text{ V} - 3 \text{ V})^2 = 0.24 \times 10^{-3}(9)$$

$$= 2.16 \text{ mA}$$

For $V_{GS} = 10 \text{ V}$ (slightly greater than $V_{GS(\text{Th})}$):

$$I_D = 0.24 \times 10^{-3}(10 \text{ V} - 3 \text{ V})^2 = 0.24 \times 10^{-3}(49)$$

$$= 11.76 \text{ mA}$$

For the Network Bias Line:

$$V_{GS} = V_{DD} - I_D R_D$$

$$= 12 \text{ V} - 2 \text{ mA}(2 \text{ k} \Omega)$$

$$V_{GS} = V_{DD} = 12 \text{ V}$$

$$I_D = \frac{V_{DD}}{R_n} = \frac{12 \text{ V}}{2 \text{ k} \Omega} = 6 \text{ mA}$$

$$V_{GS} = 0 \text{ V}$$

$I_D = 2.75 \text{ mA}$

$V_{GS0} = 6.4 \text{ V}$

$V_{DS0} = V_{GS0} = 6.4 \text{ V}$

Voltage-Divider Biasing Arrangement

Applying KVL around the indicated loop of fig8-41 will result:

$$+V_G - V_{GS} - R_2 = 0$$

$$V_{GS} = V_G - V_{R_2}$$
Example 12: Determine $I_{DQ}$, $V_{GSQ}$, and $V_{DS}$ for the network of fig8-42

**Solution: Network:**

\[
V_G = \frac{R_3 V_{DD}}{R_1 + R_3} = \frac{(18 \, \text{M} \Omega)(40 \, \text{V})}{22 \, \text{M} \Omega + 18 \, \text{M} \Omega} = 18 \, \text{V}
\]

\[
V_{GS} = V_G - I_D R_S = 18 \, \text{V} - I_D(0.82 \, \text{k} \Omega)
\]

When $I_D = 0 \, \text{mA}$

\[
V_{GS} = 18 \, \text{V} - (0 \, \text{mA})(0.82 \, \text{k} \Omega) = 18 \, \text{V}
\]

As appearing on fig 8-43, when $V_{GS} = 0 \, \text{V}$

\[
V_G = 18 \, \text{V} - I_D(0.82 \, \text{k} \Omega)
\]

\[
0 = 18 \, \text{V} - I_D(0.82 \, \text{k} \Omega)
\]

\[
I_D = \frac{18 \, \text{V}}{0.82 \, \text{k} \Omega} = 21.95 \, \text{mA}
\]

Device:

\[
V_{GS(th)} = 5 \, \text{V}, \quad I_{D(on)} = 3 \, \text{mA} \text{ with } V_{GS(on)} = 10 \, \text{V}
\]

\[
k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(th))})^2}
\]

\[
k = \frac{3 \, \text{mA}}{(10 \, \text{V} - 5 \, \text{V})^2} = 0.12 \times 10^{-4} \, \text{A/V}^2
\]

\[
I_D = k(V_G - V_{GS(th)})^2
\]

\[
= 0.12 \times 10^{-4}(V_G - 5)^2
\]

\[
I_{DQ} = 6.7 \, \text{mA}
\]

\[
V_{GSQ} = 12.5 \, \text{V}
\]

\[
V_{DS} = V_{DD} - I_D(R_S + R_D)
\]

\[
= 40 \, \text{V} - (6.7 \, \text{mA})(0.82 \, \text{k} \Omega + 3.0 \, \text{k} \Omega)
\]

\[
= 40 \, \text{V} - 25.6 \, \text{V}
\]

\[
= 14.4 \, \text{V}
\]
SUMMARY

1- A fixed-bias configuration has, a fixed dc voltage applied from gate to source to establish the operating point.

2- The nonlinear relationship between the gate-to-source voltage and the drain current of a JFET requires that a graphical or mathematical solution be used to determine the quiescent point of operation.

3- All voltages with a single subscript define a voltage from a specified point to ground.

4- The self-bias configuration is determined by an equation for $V_{GS}$ that will always pass through the origin. Any other point determined by the biasing equation will establish a straight line to represent the biasing network.

5- For the voltage-divider biasing configuration, one can always assume that the gate current is 0A to permit isolation or the voltage-divider network from the output section. The resulting gate-to-ground voltage will always be positive for an n-channel JFET and negative for a p-channel JFET. Increasing values of $R_s$ result in lower quiescent values of $I_D$ and more negative values of $V_{GS}$ for an n-channel JFET.

6- The method of analysis applied to depletion-type MOSFETs is the same as applied to JFETs, with the only difference being a possible operating point with an $I_D$ level above the $I_{DSS}$ value.

7- The characteristics and method of analysis applied to enhancement-type MOSFETs are entirely different from those of JFETs and depletion-type MOSFETs. For values of $V_{GS}$ less than the threshold value, the drain current $I_D$ is 0A.

8- When analyzing networks with a variety of devices. First work with the region of the network that will provide a voltage or current level using the basic relationships associated with those devices. Then use that level and the appropriate equations to find other voltage or current levels of the network in the surrounding region of the system.

9- The design process often requires finding a resistance level to establish the desired voltage or current level. With this in mind remember that a resistance level is defined by the voltage across the resistor divided by the current through the resistor. In the design process, both of these quantities are often available for a particular resistive element.

10- The analysis of p-channel FETs is the same as that applied to n-channel FETs except for the fact that all the voltages will have the opposite polarity and the currents the opposite direction.
### SUMMARY TABLE

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<th>Type</th>
<th>Configuration</th>
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| JFET Fixed-bias    | V<sub>DD</sub> | \( V_{GS} = -V_{GG} \)  
\( V_{DS} = V_{DD} - I_D R_D \) | ![Graph](image1) |
| JFET Self-bias     | \( V_{DD} \) | \( V_{GS} = -I_D R_S \)  
\( V_{DS} = V_{DD} - I_D (R_D + R_S) \) | ![Graph](image2) |
| JFET Voltage-divider bias | \( R_1 \) | \( V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \)  
\( V_{GS} = V_G - I_D R_S \)  
\( V_{DS} = V_{DD} - I_D (R_D + R_S) \) | ![Graph](image3) |
| JFET Common-gate   | \( V_{GG} \) | \( V_{GS} = V_{SS} - I_T R_S \)  
\( V_{DS} = V_{DD} + V_{SS} - I_D (R_D + R_S) \) | ![Graph](image4) |
| JFET \( V_{GS} = 0 \text{ V} \) | \( V_{DD} \) | \( V_{GS} = 0 \text{ V} \)  
\( I_{DQ} = I_{DSS} \) | ![Graph](image5) |
| JFET \( R_D = 0 \text{ \Omega} \) | \( R_G \) | \( V_{GS} = -I_D R_S \)  
\( V_D = V_{DD} \)  
\( V_S = I_D R_S \)  
\( V_{DS} = V_{DD} - I_S R_S \) | ![Graph](image6) |
| Depletion-type MOSFET Fixed-bias | \( V_{GG} \) | \( V_{GS} = +V_{GG} \)  
\( V_{DS} = V_{DD} - I_D R_S \) | ![Graph](image7) |
| Depletion-type MOSFET Voltage-divider bias | \( V_{DD} \) | \( V_G = \frac{R_2 V_{DD}}{R_1 - R_2} \)  
\( V_{GS} = V_G - I_D R_S \)  
\( V_{DS} = V_{DD} - I_D (R_D - R_S) \) | ![Graph](image8) |
Equations:

JFETs/depletion-type MOSFETs:

Fixed-bias configuration: \( V_{GS} = -V_{GG} = V_G \)
Self-bias configuration: \( V_{GS} = -I_D R_S \)
Voltage-divider biasing: \( V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \)
\( V_{GS} = V_G - I_D R_S \)

Enhancement-type MOSFETs:

Feedback biasing: \( V_{DS} = V_{GS} \)
\( V_{GS} = V_{DD} - I_D R_D \)
Voltage-divider biasing: \( V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \)
\( V_{GS} = V_G - I_D R_S \)
9-FET Small signal analysis

The gate-to-source ac voltage controls the drain-to-source (channel) current of an FET, Skockley's equation controlled the level of dc drain current through a relationship

\[ I_D = I_{DS} \left( 1 - \frac{V_{GS}}{V_P} \right) \]

\( g_m \) is a trans-conductance factor using to determined The change in Drain current that will result from a change in gate-to-source voltage in the following:

\[ \Delta I_D = g_m \Delta V_{GS} \]

Conductance of resistor \( g = 1/R = I/V \)

\[ g_m = \frac{\Delta I_D}{\Delta V_{GS}} \]  

[9-1]

Graphical Determination of \( g_m \)

\[ g_m = m = \frac{\Delta y}{\Delta x} = \frac{\Delta I_D}{\Delta V_{GS}} \]  

[9-2]

![Graph 9-1: Definition of \( g_m \) using transfer characteristic](image)

**Example 1:** Determine \( g_m \) for the JFET with \( I_{DSS} = 8\,mA \) & \( V_P = -4 \) at the following dc bias point: (a) \( V_{GS} = -0.5V \), (b) \( V_{GS} = -1.5V \), (c) \( V_{GS} = -2.5V \)

**Solution:**

\[ g_m = \frac{\Delta I_D}{\Delta V_{GS}} \]

(a) \( g_m = \frac{2.1\,mA}{0.6\,V} = 3.5\,mS \)

(b) \( g_m = \frac{1.8\,mA}{0.7\,V} = 2.57\,mS \)

(c) \( g_m = \frac{1.5\,mA}{1.0\,V} = 1.5\,mS \)

![Graph 9-2: Calculating \( g_m \) at various bias points](image)
Mathematical Definition of $g_m$

The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.

$$g_m = rac{\Delta I_D}{\Delta V_{GS}}_{\text{Q-pt.}} = \left. \frac{dI_D}{dV_{GS}} \right|_{\text{Q-pt.}} = \frac{d}{dV_{GS}} \left[ I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 \right]$$

$$= I_{DSS} \frac{d}{dV_{GS}} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 = 2I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right] \frac{d}{dV_{GS}} \left( 1 - \frac{V_{GS}}{V_P} \right)$$

$$= 2I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right] \frac{d}{dV_{GS}} \frac{1}{V_P} - \frac{1}{V_P} \frac{dV_{GS}}{dV_{GS}} = 2I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right] \left[ 0 - \frac{1}{V_P} \right]$$

$$g_m = \frac{2I_{DSS}}{|V_P|} \left[ 1 - \frac{V_{GS}}{V_P} \right]$$

The maximum value of $g_m$ for a JFET in which $I_{DSS}$ and $V_P$ have been specified

$$g_m = \frac{2I_{DSS}}{|V_P|} \left[ 1 - \frac{0}{V_P} \right]$$

$0$ means the value of $g_m$ when $V_{GS} = 0$ V, Eq[9-4] then becomes

$$g_m = \frac{2I_{DSS} V_P}{V_P^2} \left[ 1 - \frac{V_{GS}}{V_P} \right]$$

**Example 2:** For the JFET having the transfer char-of Ex1:

(a) find the maximum value of $g_m$

(b) find the value of $g_m$ at each operating point of Ex1: using Eq[9-6] and compare with graphical result

**Solution:**

a) $g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8 \text{ mA})}{4 \text{ V}} = 4 \text{ mS}$ (maximum possible value of $g_m$)

b) At $V_{GS} = -0.5 \text{ V},$

$$g_m = g_{m0} \left[ 1 - \frac{V_{GS}}{V_P} \right] = 4 \text{ mS} \left[ 1 - \frac{-0.5 \text{ V}}{-4 \text{ V}} \right] = 3.5 \text{ mS}$$

At $V_{GS} = -1.5 \text{ V},$

$$g_m = g_{m0} \left[ 1 - \frac{V_{GS}}{V_P} \right] = 4 \text{ mS} \left[ 1 - \frac{-1.5 \text{ V}}{-4 \text{ V}} \right] = 2.5 \text{ mS}$$

At $V_{GS} = -2.5 \text{ V},$

$$g_m = g_{m0} \left[ 1 - \frac{V_{GS}}{V_P} \right] = 4 \text{ mS} \left[ 1 - \frac{-2.5 \text{ V}}{-4 \text{ V}} \right] = 1.5 \text{ mS}$$
On specification sheet, \( g_m \) is provided as \( y_{fs} \) where \( y \) indicates it is part of an admittance equivalent circuit. The \( f \) signifies forward transfer parameter, and the \( s \) reveals that it is connected to the source terminal. In equation:

\[
g_m = y_{fs}
\]

**Plotting \( g_m \) vs. \( V_{GS} \):** Eq [9-6], When \( V_{GS} = 1/2V_P \), \( g_m \) will be 1/2 the maximum value (\( g_{m0} \))

**Example 3:** Plot \( g_m \) vs. \( V_{GS} \) for the JFET of Ex 1: and Ex 2:

**Solution:**

**Impact of \( I_D \) on \( g_m \):**

Substituting Eq[9-8] into Eq.[9-6] will result in:

\[
g_m = g_{m0} \left( 1 - \frac{V_{GS}}{V_P} \right) = g_{m0} \sqrt{\frac{I_D}{I_{DSS}}}
\]

(a) If \( I_D = I_{DSS} \),

\[
g_m = g_{m0} \sqrt{I_{DSS}} = g_{m0}
\]

(b) If \( I_D = I_{DSS}/2 \),

\[
g_m = g_{m0} \sqrt{\frac{I_{DSS}/2}{I_{DSS}}} = 0.707g_{m0}
\]

(c) If \( I_D = I_{DSS}/4 \),

\[
g_m = g_{m0} \sqrt{\frac{I_{DSS}/4}{I_{DSS}}} = \frac{g_{m0}}{2} = 0.5g_{m0}
\]
Example 4: Plot $I_D$ vs. $g_m$ for the JFET of Ex 1: through Ex 3:

Solution:

Fig 9-5 $g_m$ vs. $V_{GS}$, $I_{DSS} = 8mA$ & $V_P = -4V$

$$Z_{(FET)} = \infty \Omega$$  \[9-10\]

$$Z_{(FET)} = r_d = \frac{1}{g_m}$$  \[9-11\]

$$r_d = \frac{\Delta V_{GS}}{\Delta I_D} \text{, } V_{GS} \text{ constant}$$  \[9-12\]

Example 5: Determine the output impedance for the FET of fig 9-7 for $V_{GS} = 0V, -2V, 8V$

Fig 9-7 Drain char-for $r_d$ in Ex 5:
Solution: For \(V_{GS} = 0\) V, a tangent line is drawn and \(\Delta V_{DS}\) is chosen as 5 V, resulting in a \(\Delta I_D\) of 0.2 mA, substituting into Eq[9-12]

\[
r_d = \left. \frac{\Delta V_{DS}}{\Delta I_D} \right|_{V_{gs} = 0} = \frac{5 \text{ V}}{0.2 \text{ mA}} = 25 \text{ k}\Omega
\]

For \(V_{GS} = -2\) V, a tangent line is drawn and \(\Delta V_{DS}\) is chosen as 8 V, resulting in a \(\Delta I_D\) of 0.1 mA, substituting into Eq[9-12]

\[
r_d = \left. \frac{\Delta V_{DS}}{\Delta I_D} \right|_{V_{gs} = -2} = \frac{8 \text{ V}}{0.1 \text{ mA}} = 80 \text{ k}\Omega
\]

**FET ac Equivalent Circuit**

\[\text{Fig 9-8 FET ac equivalent circuit}\]

\(I_d\) control by \(V_{gs}\) is a current source \(g_m V_{gs}\) connected from drain to source to establish a 180° phase shift.

\(Z_i\) is open circuit at the input.

\(Z_o\) is \(r_d\) from drain to source.

**Example 6:** \(y_{fs} = 3.8 \text{ mS}\) and \(y_{os} = 20 \mu\text{S}\), Sketch the FET as equivalent model.

**Solution:**

\[
g_m = y_{fs} = 3.8 \text{ mS} \quad \text{and} \quad r_d = \frac{1}{y_{os}} = \frac{1}{20 \mu\text{S}} = 50 \text{ k}\Omega
\]

\[\text{Fig 9-9 FET ac model for Ex6:}\]

**1-JFET Fixed-Bias Configuration (Common-Source)**

\[\text{Fig 9-10 JFET fixed configuration}\]

\(g_m\) & \(r_d\) determined from the dc biasing arrangement specification sheet, \(V_{GG}\) & \(V_{DD}\) are set to zero by a short circuit equivalent.

\[\text{Fig 9-11 JFET ac equivalent}\]

Battery \(V_{GG}\) replaced by short.
For obtaining $Z_o$ Setting $V_i = 0V$, will establish $V_{gs}$ as 0V also, this result $g_mV_{gs} = 0mA$

\[ V_o = -g_m V_{gs}(r_d \parallel R_D) \]
\[ V_{gs} = V_i \]
\[ V_o = -g_m V_i(r_d \parallel R_D) \]

Phase Relationship: the negative sign in $A_v$ means 180° phase shift between IP & OP

**Example 7:** configuration of Ex1: had $V_{GSQ} = -2V$ & $I_{DQ} = 5.625$ mA, with $I_{DSS} = 10$ mA & $V_p = -8V$. The network is redrawn as fig9-13 with an applied signal $V_i$, the value of $y_{os}$ is provided as $40\mu s$. Determine (a) $g_m$ (b) $r_d$ (c) $Z_i$ (d) $Z_o$ (e) $A_v$ (f) $A_v$ ignoring the effect of $r_d$

**Solution:**

(a) $g_{m0} = \frac{2I_{DSS}}{V_p} = \frac{2(10 \text{ mA})}{8 \text{ V}} = 2.5 \text{ mS}$
\[ g_{m} = g_{m0} \left(1 - \frac{V_{GSQ}}{V_p}\right) = 2.5 \text{ mS} \left(1 - \frac{-2}{-8}\right) = 1.88 \text{ mS} \]

(b) $r_d = \frac{1}{y_{os}} = \frac{1}{40 \mu S} = 25 \text{ k} \Omega$

(c) $Z_i = R_G = 1 \text{ M} \Omega$

(d) $Z_o = R_D \parallel r_d = 2 \text{ k} \Omega \parallel 25 \text{ k} \Omega = 1.85 \text{ k} \Omega$

(e) $A_v = -g_m (R_D \parallel r_d) = -(1.88 \text{ mS})(1.85 \text{ k} \Omega) = -3.48$

(f) $A_v = -g_m R_D = -(1.88 \text{ mS})(2 \text{ k} \Omega) = -3.76$
2-JFET Self-Bias Configuration (Common-Source)

Bypassed $R_S$

Since the resulting configuration is the same as fig9-12, i.e. $Z_i$, $Z_o$ & $A_v$ will be the same

Un-bypassed $R_S$

Due to the open-circuit condition between the gate and the output network, $Z_i= R_G$

Phase Relationship: the negative sign in $A_v$ means 180° phase shift between IP & OP

\[
Z_i = R_G \\
Z_o = r_d || R_D \\
Z_o = R_D \\
A_i = -g_m (r_d || R_D) \\
A_o = -g_m R_D \quad r_o = 10 R_o
\]
Setting \( V_i = 0 \)V will result in the gate terminal being at ground potential (0V). The voltage across \( R_G \) is 0V, \( R_G \) "shorted out" of the picture. Applying KCL will result

\[
I_o + I_D = g_m V_{gs}
\]

\[
V_{gs} = -(I_o + I_D) R_s
\]

\[
I_o + I_D = -g_m (I_o + I_D) R_s = -g_m I_o R_s - g_m I_D R_s
\]

\[
I_o [1 + g_m R_s] = -I_D [1 + g_m R_s]
\]

\[
V_o = -I_o R_D
\]

\[
V_o = -(-I_o) R_D = I_o R_D
\]

If \( r_d \) is included in the network, the equivalent will appear as shown in fig9-18

We try to find an expression for \( I_o \) in terms of \( I_D \) applying KCL:

\[
I_o = g_m V_{gs} + I_{rz} - I_D
\]

\[
V_{rz} = V_o + V_{gs}
\]

\[
I_o = g_m V_{gs} + \frac{V_o + V_{gs}}{r_d} - I_D
\]

\[
I_o = \left( g_m + \frac{1}{r_d} \right) V_{gs} - \frac{I_D R_D}{r_d} - I_D \quad \text{using} \quad V_o = -I_o R_D
\]

\[
V_{gs} = -(I_D + I_o) R_S
\]

\[
I_o = -\left( g_m + \frac{1}{r_d} \right) (I_D + I_o) R_S - \frac{I_D R_D}{r_d} - I_D
\]

\[
I_o \left[ 1 + g_m R_s + \frac{R_S}{r_d} \right] = -I_D \left[ 1 + g_m R_s + \frac{R_S}{r_d} + \frac{R_D}{r_d} \right]
\]
For \( r_d \geq 10R_D \),

\[
\frac{1 + g_m R_s + \frac{R_S}{r_d}}{1 + g_m R_s + \frac{R_S + R_D}{r_d}} \approx R_D
\]

and

\[
Z_o \approx R_D
\]

\[9-25a\]

**A\_v:** for the network of fig9-18, applications of KVL on the input circuit result in:

\[
V_i - V_{gs} - V_{R_S} = 0
\]

\[
V_{gs} = V_i - I_D R_S
\]

Voltage across \( r_d \) applying KVL

\[
V_o - V_{R_S}
\]

\[
I' = \frac{V_o - V_{R_S}}{r_d}
\]

Applying KCL will result

\[
I_D = g_m V_{gs} + \frac{V_o - V_{R_S}}{r_d}
\]

Substituting for \( V_{gs} \) from above and substituting for \( V_o \) and \( V_{RS} \) we have

\[
I_D = g_m [V_i - I_D R_S] + \frac{(-I_D R_D) - (I_D R_S)}{r_d}
\]

\[
I_D \left[ 1 + g_m R_S + \frac{R_D + R_S}{r_d} \right] = g_m V_i
\]

\[
I_D = \frac{g_m V_i}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}
\]

The output voltage \( V_o \) is

\[
V_o = -I_D R_D = -\frac{g_m R_D V_i}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}
\]

\[9-25b\]
Phase Relationship: the negative sign in $A_v$ means $180^\circ$ phase shift between IP & OP.

Example 8: configuration of fig9-19 has $V_{GSQ}=-2.6$V & $I_{DQ}=2.6$mA, with $I_{DSS}=8$mA & $V_P=-6$V. The network is redrawn as fig9-20 with an applied signal $V_i$. The value of $y_{os}$ is given as $20 \, \mu S$.

Determine (a) $g_m$ (b) $r_d$ (c) $Z_i$ (d) $Z_o$ with and without $r_d$ (e) $A_v$ with and without $r_d$.

Solution:

(a) $g_m = \frac{2I_{DSS}}{V_P} = \frac{2(8 \, mA)}{6 \, V} = 2.67 \, mS$

$g_m = G_m \left( 1 - \frac{V_{GS}}{V_P} \right) = 2.67 \, mS \left( 1 - \frac{(-2.6 \, V)}{(-6 \, V)} \right) = 1.51 \, mS$

(b) $r_d = \frac{1}{y_{os}} = \frac{1}{20 \, \mu S} = 50 \, k\Omega$

(c) $Z_i = R_D = 1 \, M\Omega$

(d) With $r_d$:

$r_d = 50 \, k\Omega > 10R_D = 33 \, k\Omega$

Therefore,

$Z_o = R_D = 3.3 \, k\Omega$

If $r_d = \infty \Omega$

$Z_o = R_D = 3.3 \, k\Omega$

(e) Without $r_d$:

$$A_v = \frac{-g_mR_D}{1 + g_mR_S + \frac{R_D + R_S}{r_d}} = \frac{-(1.51 \, mS)(3.3 \, k\Omega)}{1 - (1.51 \, mS)(1 \, k\Omega) + \frac{3.3 \, k\Omega + 1 \, k\Omega}{50 \, k\Omega}}$$

$$A_v = -1.92$$

Without $r_d$:

$$A_v = \frac{-g_mR_D}{1 + g_mR_S} = \frac{-(1.51 \, mS)(3.3 \, k\Omega)}{1 + (1.51 \, mS)(1 \, k\Omega)} = -1.98$$
3-JFET Voltage-Divide Configuration (Common-Source)

The output is taken off the source terminal and when the dc supply is replaced by its short-circuit equivalent, the drain is grounded (hence, the terminology common-drain).
Fig 9.24 JFET Source-Follower configuration

Setting $V_i = 0V$ will result in the gate terminal being connected directly to ground so that $Z_o = \frac{V_o}{V_o} = -V_{gs}$ applying KCL at node S

$$I_o + g_m V_{gs} = I_{r_d} + I_{r_s}$$

$$I_o = \frac{V_o}{r_d} + \frac{V_o}{R_s}$$

$$I_o = V_o \left[ \frac{1}{r_d} + \frac{1}{R_s} \right] - g_m V_{gs}$$

$$I_o = V_o \left[ \frac{1}{r_d} + \frac{1}{R_s} \right] - g_m [-V_o]$$

$$I_o = V_o \left[ \frac{1}{r_d} + \frac{1}{R_s} + g_m \right]$$

$$Z_o = \frac{V_o}{I_o} = \frac{V_o}{r_d + \frac{1}{R_s} + g_m} = \frac{1}{r_d + \frac{1}{R_s} + g_m}$$

$$Z_o = r_d |R_s| 1/g_m$$
Applying KVL around the perimeter of the network of fig 9-26 will result in:

\[ V_i = V_{gs} + V_o \]
\[ V_{gs} = V_i - V_o \]
\[ V_o = g_m(V_i - V_o)(r_d || R_s) \]
\[ V_o = g_m V_i(r_d || R_s) - g_m V_o(r_d || R_s) \]
\[ V_o[1 + g_m(r_d || R_s)] = g_m V_i(r_d || R_s) \]

\[ A_v = \frac{V_o}{V_i} = \frac{g_m(r_d || R_s)}{1 + g_m(r_d || R_s)} \]

Since the bottom of Eq[9-37] is larger than the numerator by a factor of one, the gain can never be equal to or greater than one.

**Phase Relationship:** since \( A_v \) is a positive quantity, \( V_o \) and \( V_i \) are in phase.

**Example 9:** A dc analysis of fig 9-27 will result in \( V_{GSQ} = -2.86 \text{V} \) & \( I_{DQ} = 4.56 \text{mA} \). Determine (a) \( g_m \) (b) \( r_d \) (c) \( Z_i \) (d) \( Z_o \) with and without \( r_d \) (e) \( A_v \) with and without \( r_d \)

**Solution:**

a) \( g_{ds} = \frac{2I_{DSS}}{|V_p|} = \frac{2(16 \text{mA})}{4 \text{V}} = 8 \text{mS} \)
\[ g_m = g_m \left( 1 - \frac{V_{GSQ}}{V_p} \right) = 8 \text{mS} \left( 1 - \frac{-2.86 \text{V}}{-4 \text{V}} \right) = 2.28 \text{mS} \]

b) \( r_d = \frac{1}{g_m} = \frac{1}{25 \mu \text{S}} = 40 \text{kΩ} \)

c) \( Z_i = R_i = 1 \text{MΩ} \)

d) With \( r_d \):
\[ Z_o = r_d || R_s || 1/g_m = 40 \text{kΩ} || 2.2 \text{kΩ} || 1/2.28 \text{mS} \]
\[ = 40 \text{kΩ} || 2.2 \text{kΩ} || 438.6 \text{Ω} \]
\[ = 362.52 \text{Ω} \]

Without \( r_d \):
\[ Z_o = R_s || 1/g_m = 2.2 \text{kΩ} || 438.6 \text{Ω} = 365.69 \text{Ω} \]

e) With \( r_d \):
\[ A_v = \frac{g_m(r_d || R_s)}{1 + g_m(r_d || R_s)} = \frac{(2.28 \text{mS})(40 \text{kΩ})}{1 + (2.28 \text{mS})(40 \text{kΩ})} \]
\[ = \frac{(2.28 \text{mS})(2.09 \text{kΩ})}{1 + (2.28 \text{mS})(2.09 \text{kΩ})} = 0.83 \]
Depletion-Type MOSFETs
The ac equivalent model for D-MOSFETs is exactly the same as that employed for JFETs as shown in fig9-28, the only difference is that $V_{GSQ}$ can be positive for n-channel and negative for p-channel devices, the result is that $g_m$ can be greater than $g_{m0}$

![Fig9-28 D-MOSFET ac circuit](image)

**Example 10:** The network of fig9-29 was analyzed, resulting in $V_{GSQ} = 0.35V \ \& \ I_{DQ} = 7.6mA$, Determine (a) $g_m$ and compare to $g_{m0}$ (b) $r_d$ (c) Sketch the ac equivalent network (d) $Z_i$ (e) $Z_o$ (f) $A_v$

**Solution:**

(a) $g_{sc} = \frac{2I_{DSS}}{V_{DS}} = \frac{2(6 \ mA)}{3V} = 4 \ mS$

$$g_m = g_{sc}(1 - \frac{V_{GSQ}}{V_{P}}) = 4 \ mS \left(1 - \frac{0.35 \ V}{-3 \ V}\right) = 4.47 \ mS(1 - 0.117) = 4.47 \ mS$$

(b) $r_d = \frac{1}{g_{sc}} = \frac{1}{10 \ \mu S} = 100 \ k\Omega$

![Fig9-29 network for Ex10](image)

(C) See fig9-30 the similarities with the network of JFET fixed bias, self bias (bypassed) & voltage divider configuration so that the same Equation applied

**Enhancement-Type MOSFETs**
For the E-MOSFETs, the relationship between output current and controlling voltage is

$$I_D = k(V_{GS} - V_{GS(Th)})^2$$

Without $r_d$:

$$A_v = \frac{g_mR_S}{1 + g_mR_S} = \frac{(2.28 \ mS)(2.2 \ k\Omega)}{1 + (2.28 \ mS)(2.2 \ k\Omega)} = \frac{5.02}{1 + 5.02} = 0.83$$

**Fig9-30 ac equivalent**
\[ g_m = \frac{\Delta I_D}{\Delta V_{GS}} \]

\[ g_m = 2k(V_{GS} - V_{GS(Th)}) \]

Can be determined from a given typical operating point on a specification sheet

1- E-MOSFET Voltage Divider Configuration

\[ Z_i = R_1 || R_2 \]

\[ Z_o = r_d || R_D \]

\[ Z_o = R_d \quad r_d \geq 10R_o \]

\[ A_v = V_o = -g_m (r_d || R_D) \]

\[ A_v = \frac{V_o}{V_i} = -g_m R_D \]
Designing FET Amplifier Network

Example 12: Design the fixed-bias network of fig9-34 to have an ac gain of 10, that is determining the value of $R_D$

![Fig 9-34 circuit for desired voltage gain in Ex11:](image)

Solution:

$V_{G\text{e}} = 0$ V, the level of $g_m$ is $g_{m0}$. The gain is therefore determined by

$$
A_v = -\frac{g_m}{r_d} = -\frac{g_{m0}}{r_d} = \frac{2I_{DSST}}{|V_P|} = \frac{2(10 \text{ mA})}{4 \text{ V}} = 5 \text{ mS}
$$

$$
-10 = -\frac{5 \text{ mS} \cdot R_D}{r_d}
$$

$$
R_D \cdot r_d = \frac{10}{5 \text{ mS}} = 2 \text{ k}\Omega
$$

$$
r_d = \frac{1}{Y_{m0}} = \frac{1}{20 \times 10^{-6} \text{ S}} = 50 \text{ k}\Omega
$$

$$
R_D \cdot r_d = 2 \text{ k}\Omega
$$

$$
\frac{R_D(50 \text{ k}\Omega)}{R_D + 50 \text{ k}\Omega} = 2 \text{ k}\Omega
$$

$$
50R_D = 2(R_D + 50 \text{ k}\Omega) = 2R_D + 100 \text{ k}\Omega
$$

$$
48R_D = 100 \text{ k}\Omega
$$

$$
R_D = \frac{100 \text{ k}\Omega}{48} = 2.08 \text{ k}\Omega
$$

The closest standard value is 2KΩ, which would be employed for this region, the resulting level of $V_{DSQ}$ would then be determined as follows:

$$
V_{DSQ} = V_{DD} - I_D r_d = 30 \text{ V} - (10 \text{ mA})(2 \text{ k}\Omega) = 10 \text{ V}
$$

$Z_i$ and $Z_o$ are set by the levels of $R_i$ and $R_D$, respectively. That is,

$$
Z_i = R_i = 10 \text{ M}\Omega
$$

$$
Z_o = R_D \cdot r_d = 2 \text{ k}\Omega \cdot 50 \text{ k}\Omega = 1.92 \text{ k}\Omega \approx R_D = 2 \text{ k}\Omega
$$

Example 13: Choose the value of $R_D$ and $R_S$ for the network of fig 9-35 that will result in a gain of 8 using a relatively high level of $g_m$ for this device defined at $V_{GSQ} = 1/4 V_P$

Solution:
The closest standard value is 180Ω, in this example; Rs does not appear in the ac design because of the shorting effect of Cs.

**Example 13:** Determine $R_D$ and $R_S$ for the network of fig9-35 to establish a gain of 8 of the bypass capacitor $C_S$ is removed.

**Solution:** $V_{GSQ}$ and $I_D$ are still -1V and 5.625mA, and since the equation $V_{GS} = -I_D R_S$ has not changed, $R_S$ continues to equal the standard value of 180Ω.

$$A_V = \left| g_m \left( R_D || r_d \right) \right|$$

|8| = \left| \frac{-(3.75 \text{ mS})R_D}{1 + (3.75 \text{ mS})(180 \Omega)} \right| = \frac{(3.75 \text{ mS})R_D}{1 + 0.675} = \frac{13.4}{3.75 \text{ mS}} = 3.573 \text{ kΩ}$$

With the closest standard value at 3.6kΩ, we can now test the condition:

$$r_d \geq 10(R_D + R_S)$$

50 kΩ ≥ 10(3.6 kΩ + 0.18 kΩ) = 10(3.78 kΩ)

50 kΩ ≥ 37.8 kΩ
### SUMMARY TABLE

<table>
<thead>
<tr>
<th>Configuration</th>
<th>$Z_1$</th>
<th>$Z_0$</th>
<th>$A = \frac{Z_0}{Z_1}$</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Fixed-bias</strong></td>
<td>High (10 MΩ)</td>
<td>Medium (2 kΩ)</td>
<td>Medium (−10)</td>
</tr>
<tr>
<td>[JFET or D-MOSFET]</td>
<td>$V_{DD}$ $\rightarrow$ $V_o$</td>
<td>$R_D$ $\parallel R_{g5}$</td>
<td>$-\frac{g_m(V_2)R_{g5}}{R_D}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_D$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$g_m(V_2) R_D$</td>
<td></td>
</tr>
</tbody>
</table>

| **Self-bias**                 | High (10 MΩ)               | Medium (2 kΩ)               | Medium (−10)           |
| [JFET or D-MOSFET]            | $V_{DD}$ $\rightarrow$ $V_o$ | $R_D$ $\parallel R_{g5}$   | $-\frac{g_m(V_2)R_{g5}}{R_D}$ |
| Bypassed $R_g$                |                            | $R_D$                       |                        |
|                              |                            | $g_m(V_2) R_D$   |                        |

| **Self-bias**                 | High (10 MΩ)               | Medium (2 kΩ)               | Medium (−10)           |
| [JFET or D-MOSFET]            | $V_{DD}$ $\rightarrow$ $V_o$ | $R_D$ $\parallel R_{g5}$   | $-\frac{g_m(V_2)R_{g5}}{R_D}$ |
| Unbypassed $R_g$              |                            | $R_D$                       |                        |
|                              |                            | $g_m(V_2) R_D$   |                        |

| **Voltage-divider bias**      | High (10 MΩ)               | Medium (2 kΩ)               | Medium (−10)           |
| [JFET or D-MOSFET]            | $V_{DD}$ $\rightarrow$ $V_o$ | $R_D$ $\parallel R_{g5}$   | $-\frac{g_m(V_2)R_{g5}}{R_D}$ |
|                               |                            | $R_D$                       |                        |
|                               |                            | $g_m(V_2) R_D$   |                        |
1- The trans-conductance parameter $g_m$ is determined by the ratio of the change in drain current associated with a particular change in gate-to-source voltage.

2- On specification sheets, $g_m$ is provided as $y_{fs}$. 

3- When $V_{GS}$ is one-half the pinch-off value; $g_m$ is one-half the maximum value.

4- When $I_D$ is one-fourth the saturation level of $I_{DSS}$, $g_m$ is one-half the value at saturation.

5- The output impedance of FETs is similar in magnitude to that of conventional BJTs.

6- On specification sheets the output impedance $r_d$ is provided as $1/y_{os}$.

7- The voltage gain for the fixed-bias and self-bias JFET configurations (with a by-passed source capacitance) is the same.

8- The ac analysis of JFETs and depletion-type MOSFETs is the same.

9- The ac equivalent network for E-MOSFETs is the same as that employed for the JFETs and D-MOSFETs, the only difference is the equation for $g_m$.

10- The magnitude of the gain of FET networks is typically between 2 and 20. The self-bias configuration (without a by-pass source capacitance) and the source follower are low-gain configurations.

11- There is no phase shift between input and output for the source-follower.

12- The output impedance for most FET configurations is determined primarily by $R_D$. For the source-follower configuration it is determined by $R_S$ and $g_m$. 

Important Conclusion and Concept
Equations

\[ g_m = y_{\pi} = \frac{\Delta I_D}{\Delta V_{GS}} \]

\[ g_{m0} = \frac{2I_{DSS}}{V_P} \]

\[ g_m = g_{m0} \left( 1 - \frac{V_{GS}}{V_P} \right) \]

\[ g_m = g_{m0} \sqrt{\frac{I_D}{I_{DSS}}} \]

\[ r_d = \frac{1}{y_{\pi}} = \frac{\Delta V_{DS}}{\Delta I_D} \left|_{V_{in}=\text{constant}} \right. \]

JFETs and depletion-type MOSFETs \((r_d \geq 10R_D, r_d \geq 10R_S)\):

**Fixed-bias:**

\[ Z_i = R_G \]
\[ Z_o \equiv R_D \]
\[ A_v = -g_m R_D \]

**Self-bias (bypassed \(R_S\)):**

\[ Z_i = R_G \]
\[ Z_o = R_D \]
\[ A_v = -g_m R_D \]

**Self-bias (unbypassed \(R_S\)):**

\[ Z_i = R_G \]
\[ Z_o = R_D \]
\[ A_v = -\frac{g_m R_D}{1 + g_m R_S} \]

**Voltage-divider bias:**

\[ Z_i = R_i \| R_2 \]
\[ Z_o = R_D \]
\[ A_v = -g_m R_D \]

**Source-follower:**

\[ Z_i = R_G \]
\[ Z_o = R_S \| 1/g_m \]
\[ A_v = \frac{g_m R_S}{1 + g_m R_S} \]

Enhancement-type MOSFETs \(g_m = 2k(V_{GS0} - V_{GS(Th)})\)

**Voltage-divider bias:**

\[ Z_i = R_1 \| R_2 \]
\[ Z_o \equiv R_D \]
\[ A_v = -g_m R_D \]